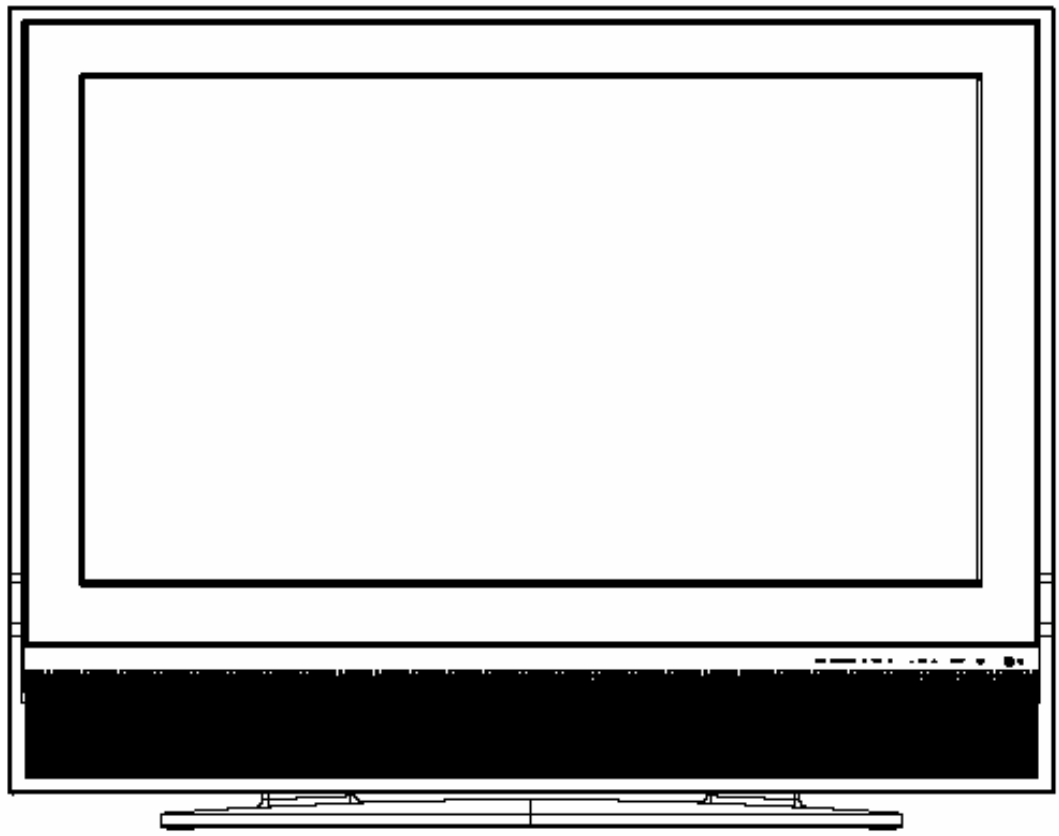
Service Manual



Model #: VIZIO VP42 HDTV20A

V, Inc

320A Kalmus Drive Costa Mesa, CA 92626

TEL : +714-668-0588 FAX :+714-668-9099

Top Confidential

Table of Contents

CONTENTS PAGE

Sections

Appendix

IBM and IBM products are registered trademarks of International Business Machines Corporation.

Macintosh and Power Macintosh are registered trademarks of Apple Computer, Inc.

VINC and VINC products are registered trademarks of V, Inc.

VESA, EDID, DPMS and DDC are registered trademarks of Video Electronics Standards Association (VESA).

Energy Star is a registered trademark of the US Environmental Protection Agency (EPA).

FCC INFORMATION
This equipment has been tested and found to comply with the limits of a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that the interference will not occur in a particular installation. If this equipment does cause unacceptable interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures -- reorient or relocate the receiving antenna; increase the separation between equipment and receiver; or connect the into an outlet on a circuit different from that to which the receiver is connected.

FCC WARNING
To assure continued FCC compliance, the user must use a grounded power supply cord and the provided shielded video interface cable with bonded ferrite cores. Also, any unauthorized changes or modifications to Amtrak products will void the user’s authority to operate this device. Thus VINC Will not be held responsible for the product and its safety.

CE CERTIFICATION
This device complies with the requirements of the EEC directive 89/336/EEC with regard to “Electromagnetic compatibility.”

SAFETY CAUTION
Use a power cable that is properly grounded. Always use the AC cords as follows – USA (UL); Canada (CSA); Germany (VDE); Switzerland (SEV); Britain (BASEC/BS); Japan (Electric Appliance Control Act); or an AC cord that meets the local safety standards.

Chapter 1 Features

1. Built in TV channel selector for TV viewing

2. Simulatnueous display of PC and TV images

3. Connectable to PC's analog RGB port

4. Built in S-video, HDTV, composite video, HDMI and TV out

5. Built in auto adjust function for automatic adjument of screen display

6. Smoothing function enables display of smooth texts and graphics even if image withresolution lower than 1024x768 is magnified

7. Picture In Picture (PIP) funtion to show TV or VCR images

8. Power saving to reduce consumption power too less than 3W

9. On Screen Display: user can define display mode (i.e. color, brightness, contrast, sharpness, backlight), sound setting, PIP, TV channel program, aspect and gamma or reset all setting.

Chapter 2 Specification

1. LCD CHARACTERISTICS

Type: PDP MODULE 42" PDP42X3 (LG)(China)(Film type)
Size: 42.02inch
Display Size: 42 inches (1067.308mm) diagonal
Outline Dimension: 1005 mm (H) x 597 mm (V) x 60.7 mm (D) (Typ.)
Pixel Pitch: 0.9mm x 0.676mm x RGB
Pixel Format: 1024 horiz. By 768 vert. Pixels RGB strip arrangement
Contrast ratio: 10000:1(Typ) (panel spec)
Luminance, White: 480 cd/m2 (Typ) (1/100 White Window)
Display Operating Mode: normally Black
Surface Treatment: Hard Coating (3H) ,Anti-glare treatment of the front polarizer.

2. OPTICAL CHARACTERISTICS

Viewing Angle
Left: free
Right: free
Top: free
Bottom: free

3. SIGNAL (Refer to the Timing Chart)

Sync Signal
1) Type: TMDS
2) Input Voltage Level: 100~240 Vac, 50/ 60 Hz

4.Input Connectors

RJ11, D-SUB15PIN (MINI, 3rows), Headphone, HDMIX2, RCAX3 (component), RCAX2 (AUDIO in), RCAX3 (composite), RCAX2 (AUDIO in), S-Video, Tuner

5. POWER SUPPLY

Power Consumption: 380W MAX
Power OFF: to less than 3W MAX

6.Speaker

Output 10W (max) X2

7. ENVIRONMENT

5-1. Operating Temperature: 5c~35c (Ambient)

5-2. Operating Humidity: 90%RH (Non-condensing)

5-3. Operating Altitude: 0 - 14,000 feet (4267.2m)(Non-Operating)

8. DIMENSIONS (Physical dimension)

Width: 1048.0 mm.

Depth: 308.0mm

Height: 757.0mm

9. WEIGHT (Physical weight)

a. Net: 33.26+/-0.5kgs

b. Gross: 40.5+/-0.5kgs

Precaution

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer.
Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former
generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizes with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene.
Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)

(2) Response time depends on the temperature. (In lower temperature, it becomes longer.)

(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(6) Module has high frequency circuits. System manufacturers shall do sufficient suppression to the electromagnetic interference. Grounding and shielding methods may be important to minimize the interference.

9-3. HANDLING PRECAUTIONS FOR PROTECTION

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

Chapter 3 On Screen Display

On Screen Display (OSD) is a friendly interface providing the function adjusting in our system. Customers could operate it only by few buttons. There is the introduction of the OSD.

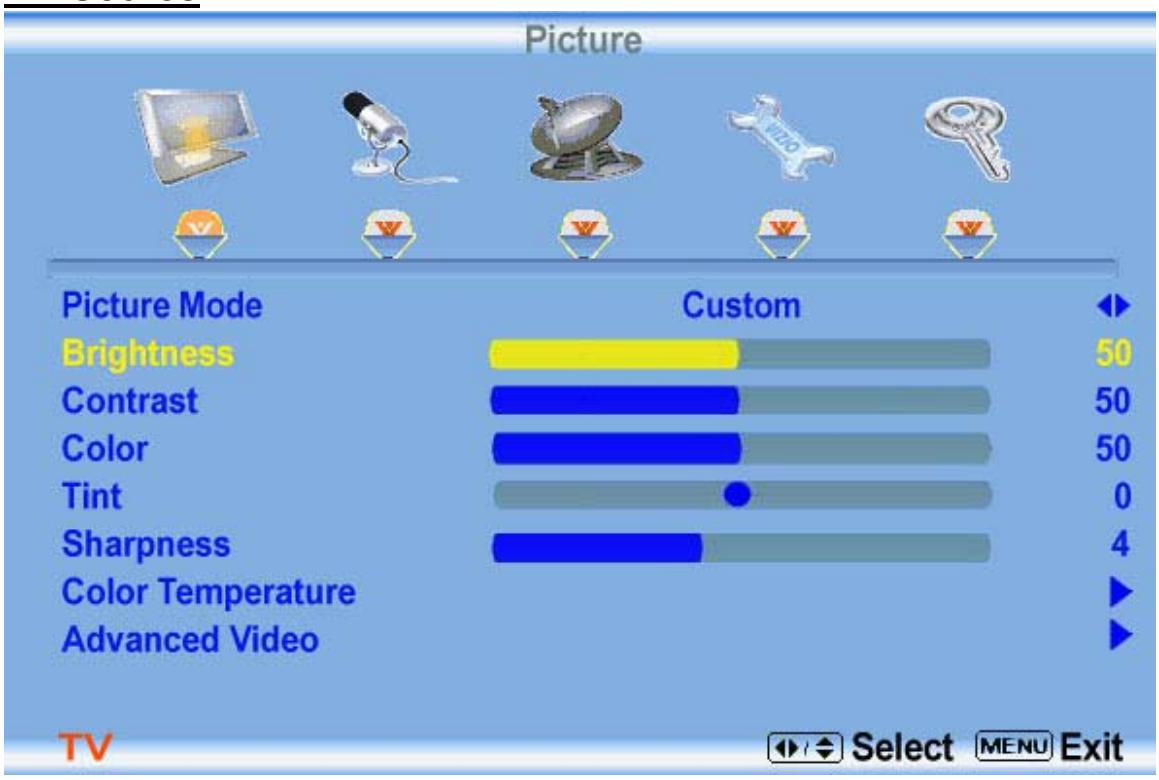
Main unit button

MENU OK
CH ▲ ↑
CH ▼ ↓
VOL + ←
VOL - →
Input

[MENU]

“MENU” button could star the OSD which could adjust the performance and set up the setting between the different input sources. There are the structures.

TV Source



A. **Picture**：(**Bold: Default**)

a. Picture Mode (Standard/Movie /Game / **Custom**)

b. Brightness (0~100, **55**)

c. Contrast (0~100, **50**)

d. Color (saturation)(0~100, **50**)

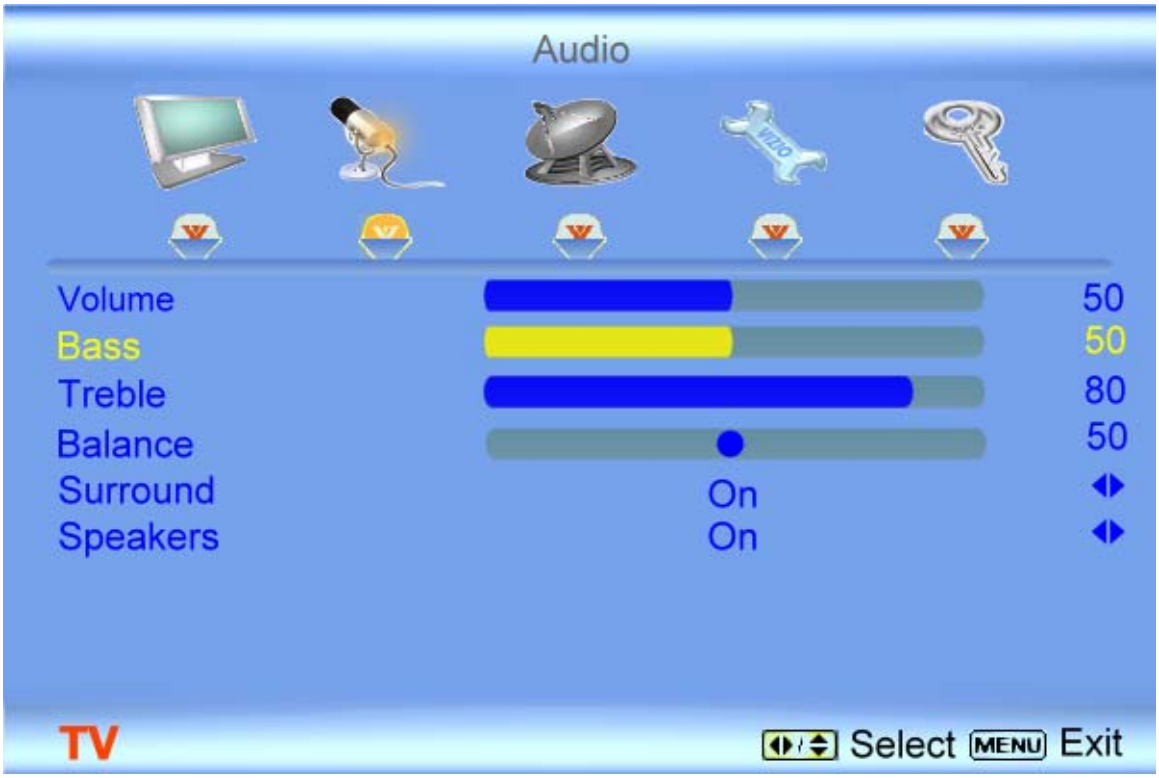
e. Tint (hue) (-32~32, **0**)

f. Sharpness (0~7, **4**)

g. Color Temperature (**Cool**/Normal/Warm/Custom)

h. Advanced Video

B. **Audio**：(**Bold: Default**)



a. Volume (0~100, **25**)

b. Bass (0~100, **50**)

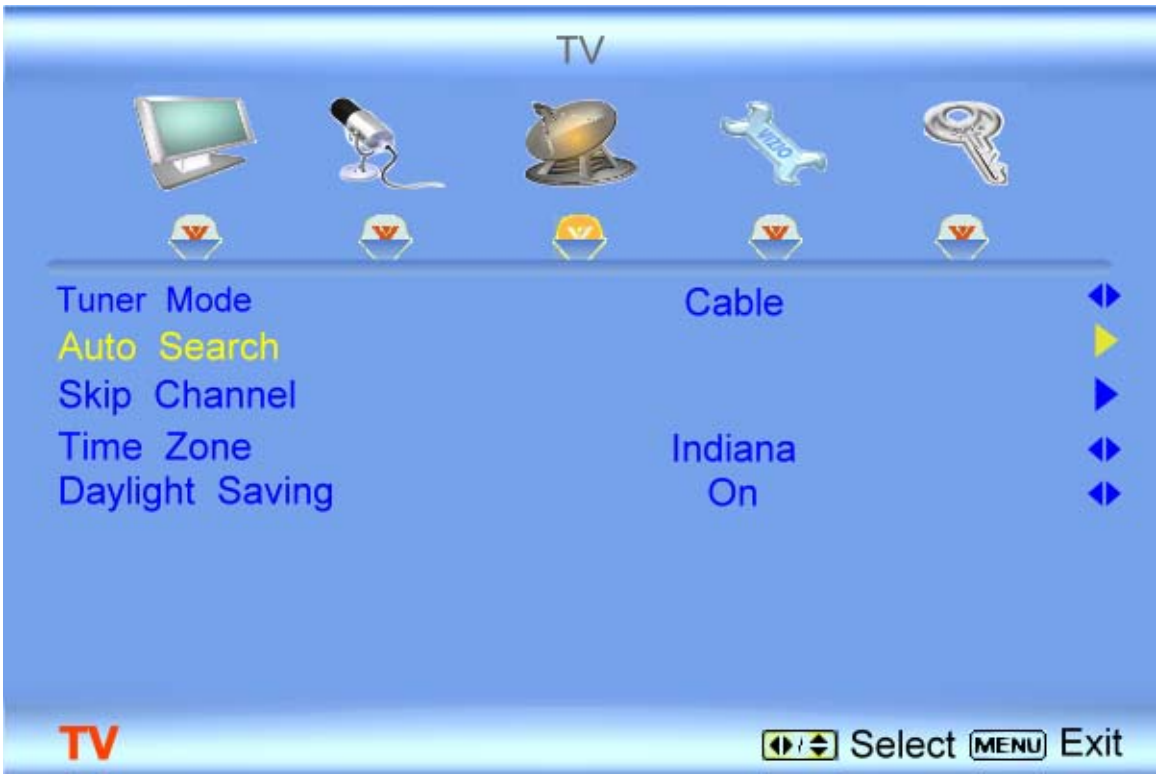
c. Treble (0~100, **50**)

d. Balance (-50~50, **0**)

e. Surround (**ON**/OFF)

f. Speakers (**ON**/OFF)

C. **TV**：(**Bold: Default**)



a. Tuner Mode (**Cable**/Air)

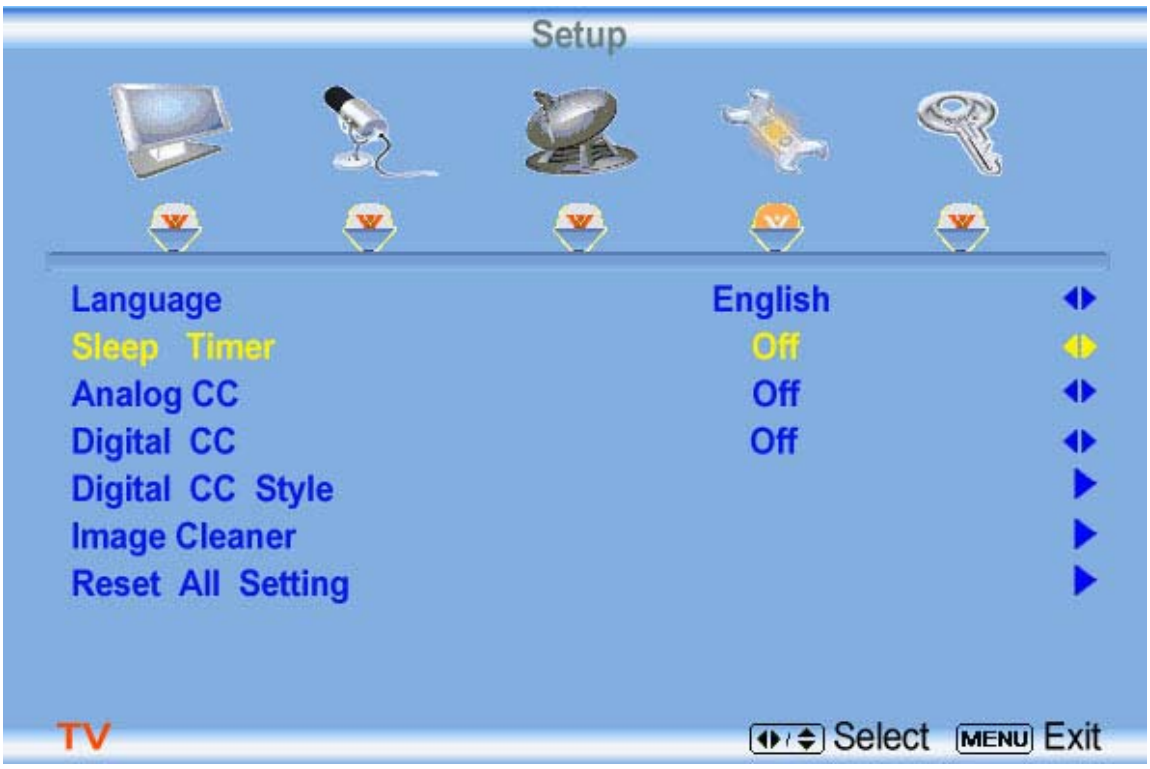
b. Auto Search

c. Skip Channel

d. Digital Audio Out (**PCM**/Dolby Digital/OFF)

e. Time Zone (**Eastern**/Indiana/Central/Mountain/Arizona/Pacific/Alaska/Hawaii)

D. **Setup**：(**Bold: Default**)



a. Language (**Englis**h/ Français / Espaňol)

b. Sleep Timer (**OFF**/30Min/60Min/90Min/120Min)

c. Analog CC (**OFF**/CC1~4/TT1~4)

d. Digital CC (**OFF**/CC1~4/Service1~6)

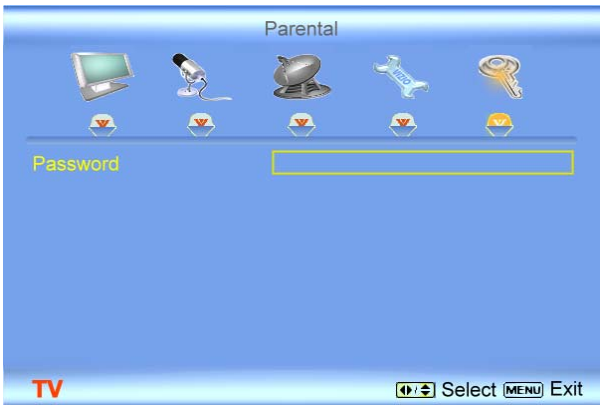
e. Digital CC Style

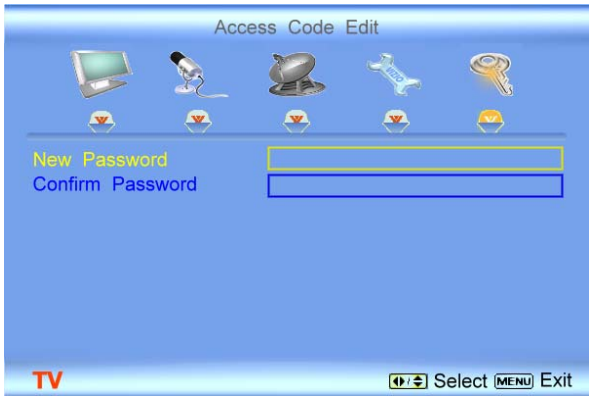
1. Caption Style (As Broadcaster/Custom)
2. Size (**Large**/Small/Medium)
3. Font Color (**White**/Green/Blue/Red/Cyan/Yellow/Magenta/Black)
4. Font Opacity (**Solid**/Translucent/Transparent)
5. Background Color (White/Green/Blue/Red/Cyan/Yellow/Magenta/**Black**)
6. Background Opacity (**Solid**/Translucent/Transparent)
7. Window Color (White/Green/Blue/Red/Cyan/Yellow/Magenta/**Black**)
8. Window Opacity (Solid/Translucent/**Transparent**)

g. Image Cleaner (ON/**OFF**)

h. Rest All Setting (OK/**Cancel**)

E. **Parental**：(**Bold: Default**)





Password (**Default => 0000**)

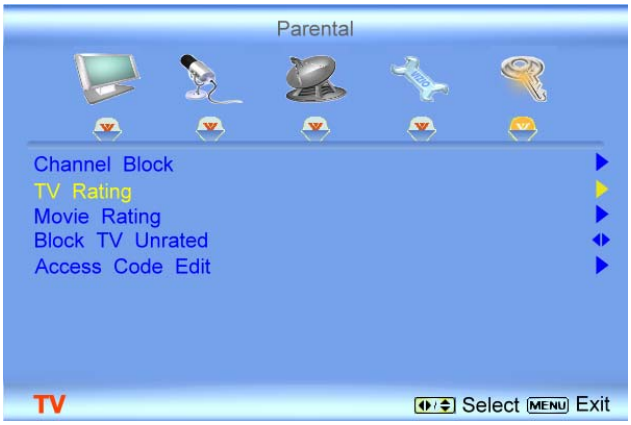
a. Cannel Block

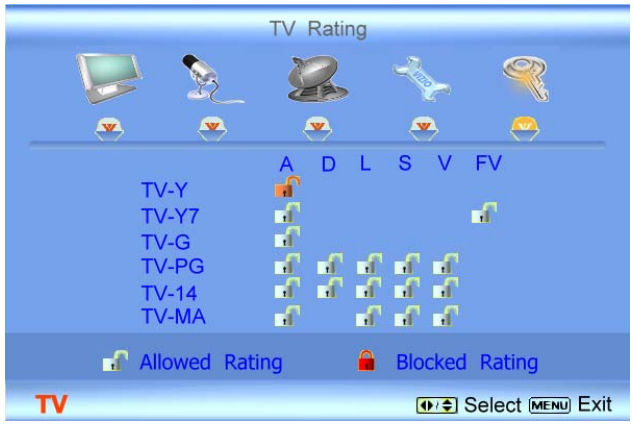
b. TV Rating

c. Move Rating

d. Block Unrated TV (**NO**/Yes)

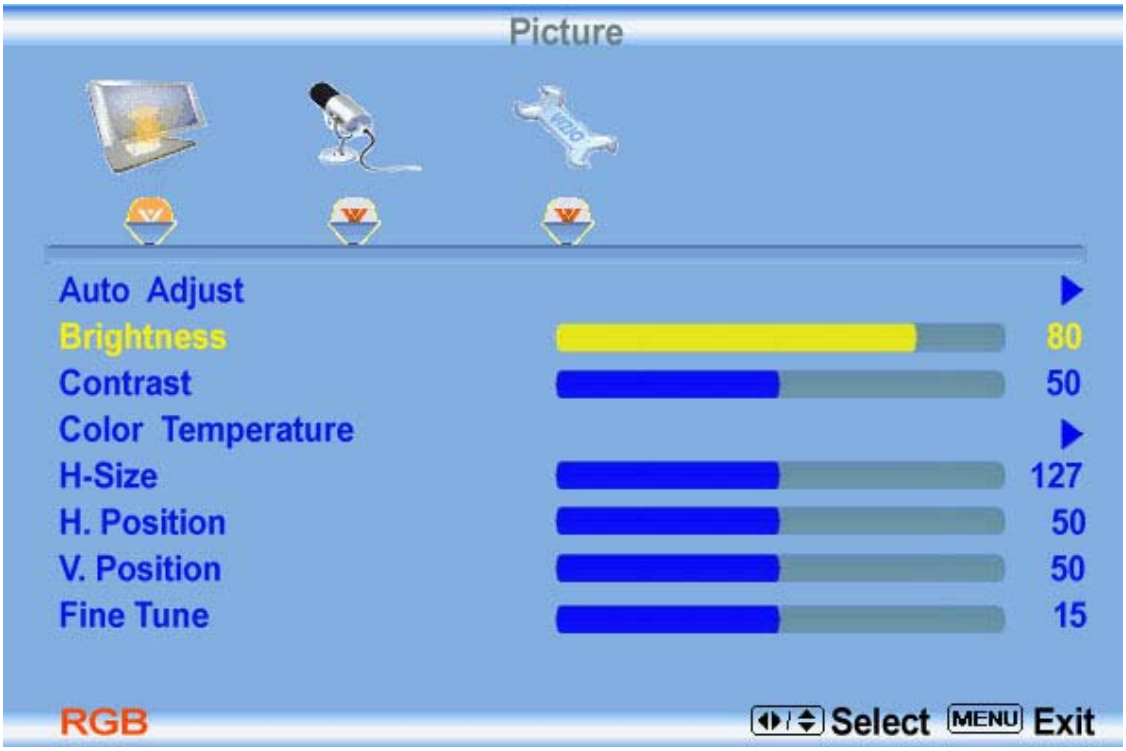
e. Access Code Edit





RGB Mode

A. Picture Adjust：(**Bold: Default**)



a. Auto Adjust

b. Brightness (0~100, **55**)

c. Contrast (0~100, **50**)

d. Color Temperature (6500/**9300**/Custom)

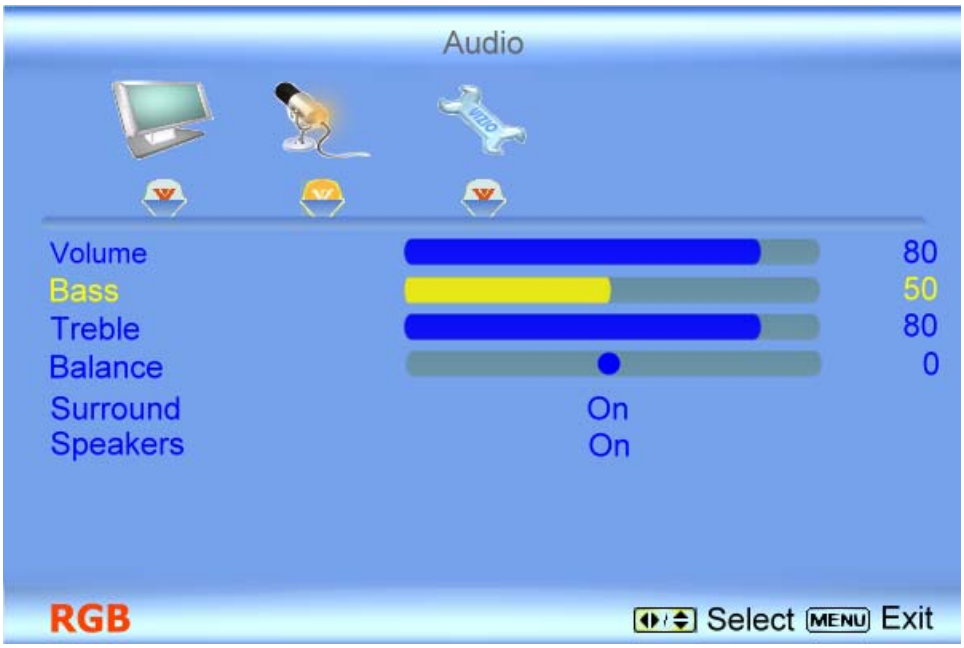
e. H-Size (0~255, **127**)

f. H-Position (0~100, **65**)

g. V-Position (0~100, **49**)

h. Fine Tune (0~31, **17**)

B. **Audio**：(**Bold: Default**)



a. Volume (0~100, **25**)

b. Bass (0~100, **50**)

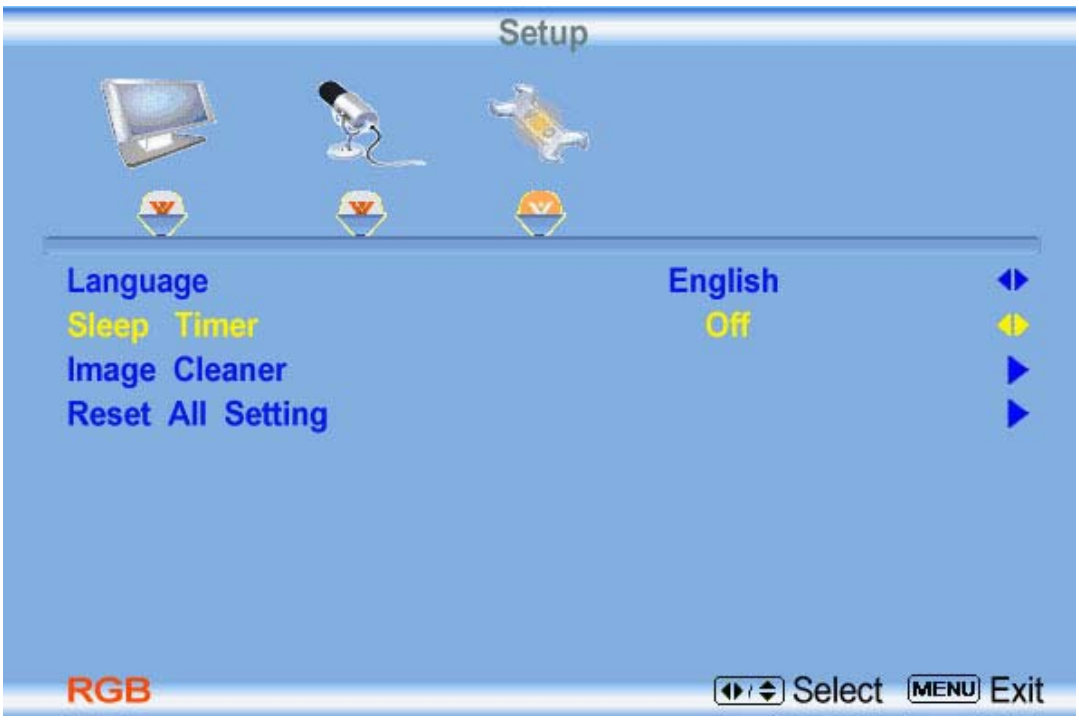
c. Treble (0~100, **50**)

d. Balance (-50~50, **0**)

e. Surround (**ON**/OFF)

f. Speakers (**ON**/OFF)

D. **Setup**：(**Bold: Default**)



a. Language (**Englis**h/ Français / Espaňol)

b. Sleep Timer (**OFF**/30Min/60Min/90Min/120Min)

c. Analog CC (**OFF**/CC1~4/TT1~4)

d. Digital CC (**OFF**/CC1~4/Service1~6)

e. Digital CC Style

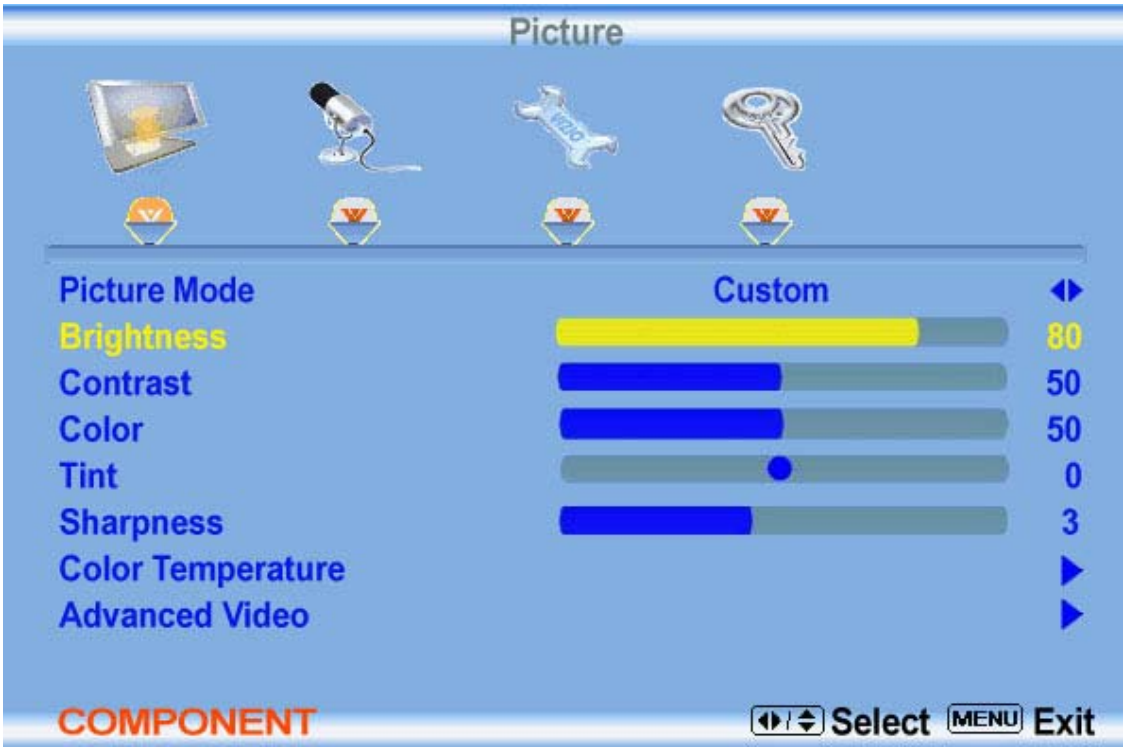
1. Caption Style (As Broadcaster/Custom)
2. Size (**Large**/Small/Medium)
3. Font Color (**White**/Green/Blue/Red/Cyan/Yellow/Magenta/Black)
4. Font Opacity (**Solid**/Translucent/Transparent)
5. Background Color (White/Green/Blue/Red/Cyan/Yellow/Magenta/**Black**)
6. Background Opacity (**Solid**/Translucent/Transparent)
7. Window Color (White/Green/Blue/Red/Cyan/Yellow/Magenta/**Black**)
8. Window Opacity (Solid/Translucent/**Transparent**)

f. Image Cleaner(ON/**OFF**)

g. Rest All Setting (OK/**Cancel**)

AV / COMPONENT MODE

A. **Picture**：(**Bold: Default**)



a. Picture Mode (Standard/Movie /Game / **Custom**)

b. Brightness (0~100, **55**)

c. Contrast (0~100, **50**)

d. Color (saturation)(0~100, **50**)

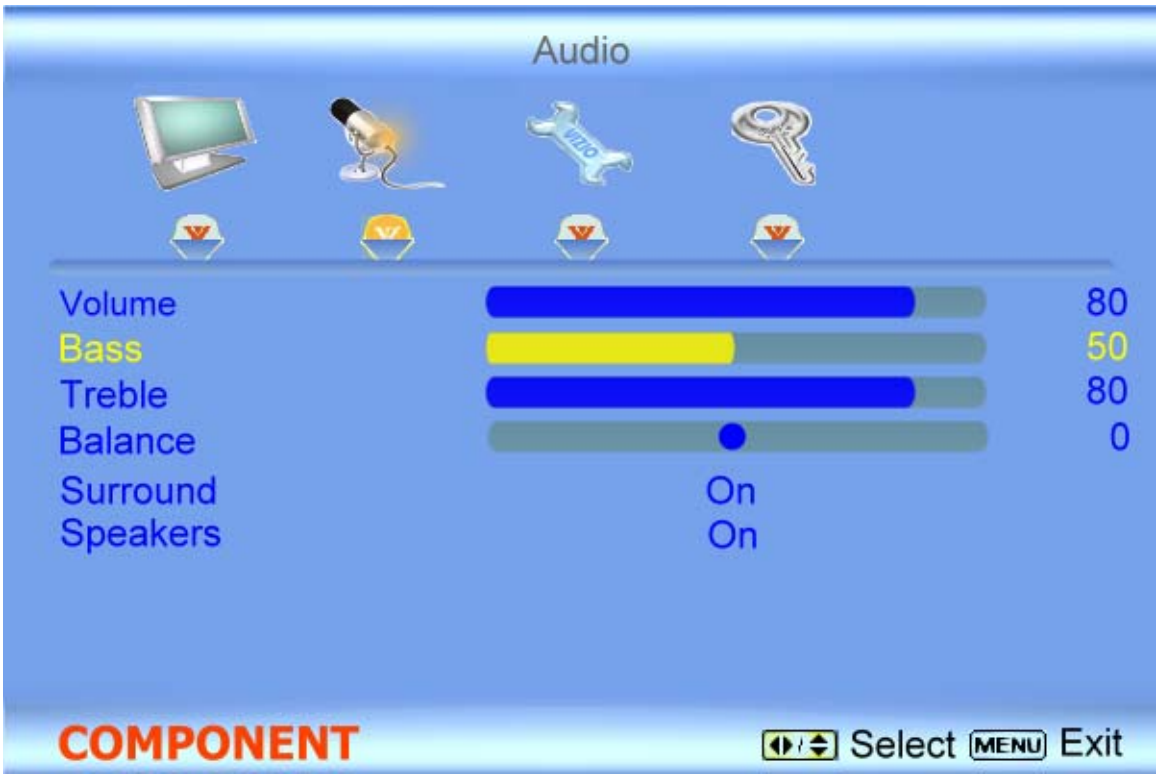
e. Tint (hue) (-32~32, **0**)

f. Sharpness (0~7, **4**)

g. Color Temperature (**Cool**/Normal/Warm/Custom)

h. Advanced Video

B. **Audio**：(**Bold: Default**)



a. Volume (0~100, **25**)

b. Bass (0~100, **50**)

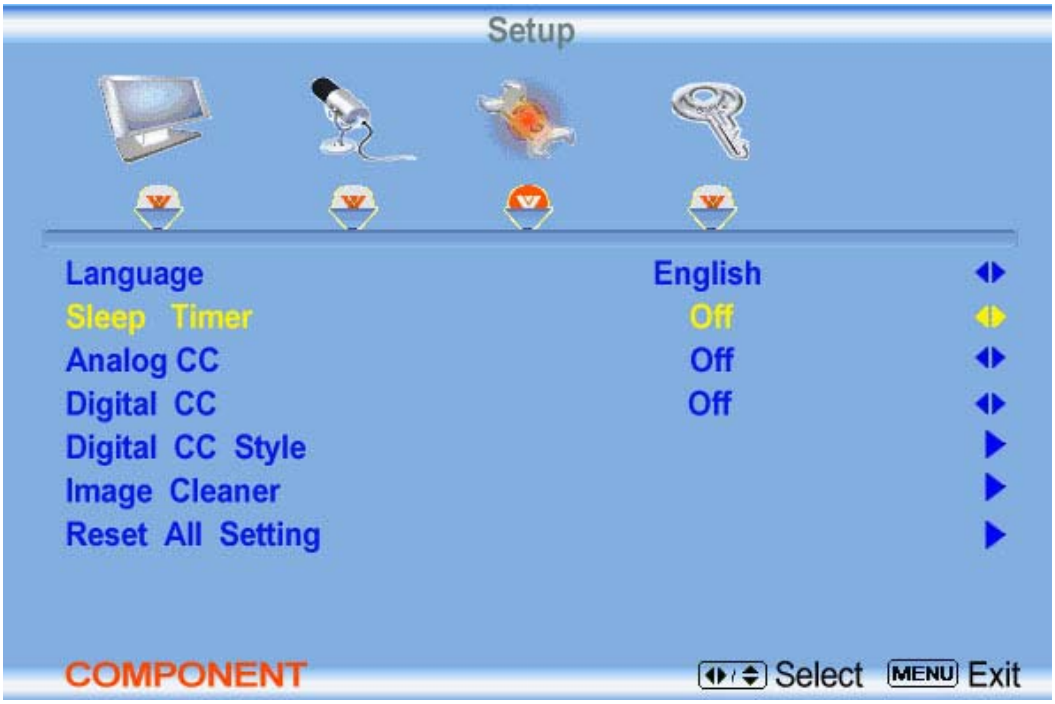
c. Treble (0~100, **50**)

d. Balance (-50~50, **0**)

e. Surround (**ON**/OFF)

f. Speakers (**ON**/OFF)

C. **Setup**：(**Bold: Default**)



a. Language (**Englis**h/ Français / Espaňol)

b. Sleep Timer (**OFF**/30Min/60Min/90Min/120Min)

c. Analog CC (**OFF**/CC1~4/TT1~4)

d. Digital CC (**OFF**/CC1~4/Service1~6)

e. Digital CC Style

1. Caption Style (As Broadcaster/Custom)
2. Size (**Large**/Small/Medium)
3. Font Color (**White**/Green/Blue/Red/Cyan/Yellow/Magenta/Black)
4. Font Opacity (**Solid**/Translucent/Transparent)
5. Background Color (White/Green/Blue/Red/Cyan/Yellow/Magenta/**Black**)
6. Background Opacity (**Solid**/Translucent/Transparent)
7. Window Color (White/Green/Blue/Red/Cyan/Yellow/Magenta/**Black**)
8. Window Opacity (Solid/Translucent/**Transparent**)

f. Image Cleaner (ON/**OFF**)

g. Rest All Setting (OK/**Cancel**)

D. **Parental**：(**Bold: Default**)

Password (**Default => 0000**)

a. Cannel Block

b. TV Rating

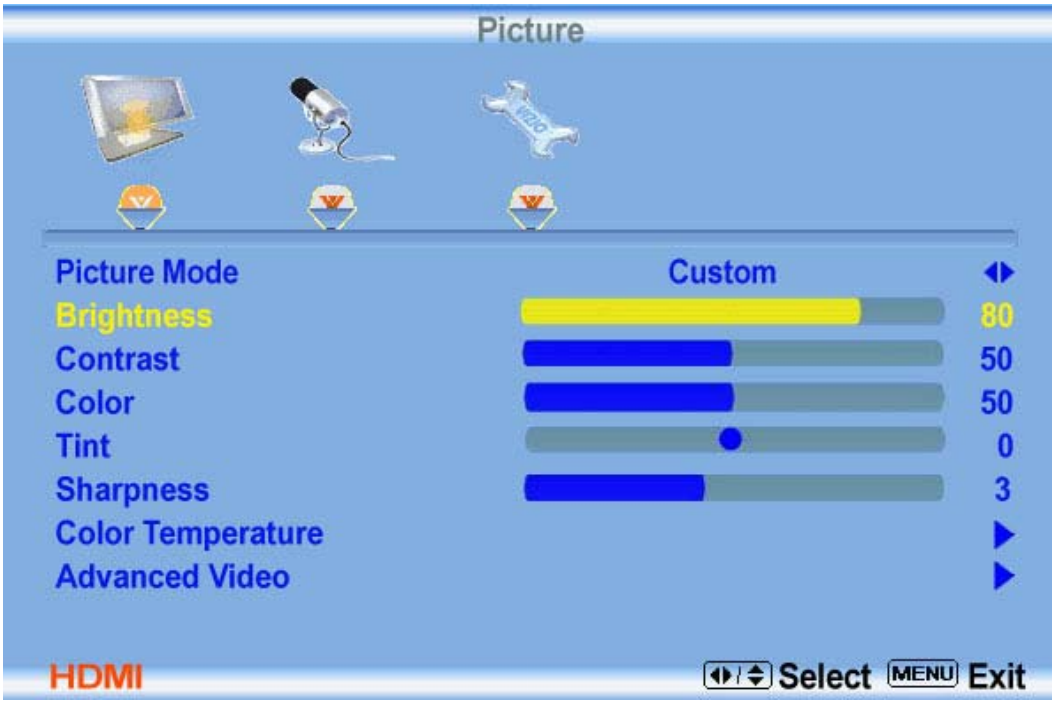
c. Move Rating

d. Block Unrated TV (**NO**/Yes)

e. Access Code Edit

HDMI MODE

A. **Picture**：(**Bold: Default**)



a. Picture Mode (Standard/Movie /Game / **Custom**)

b. Brightness (0~100, **55**)

c. Contrast (0~100, **50**)

d. Color (saturation)(0~100, **50**)

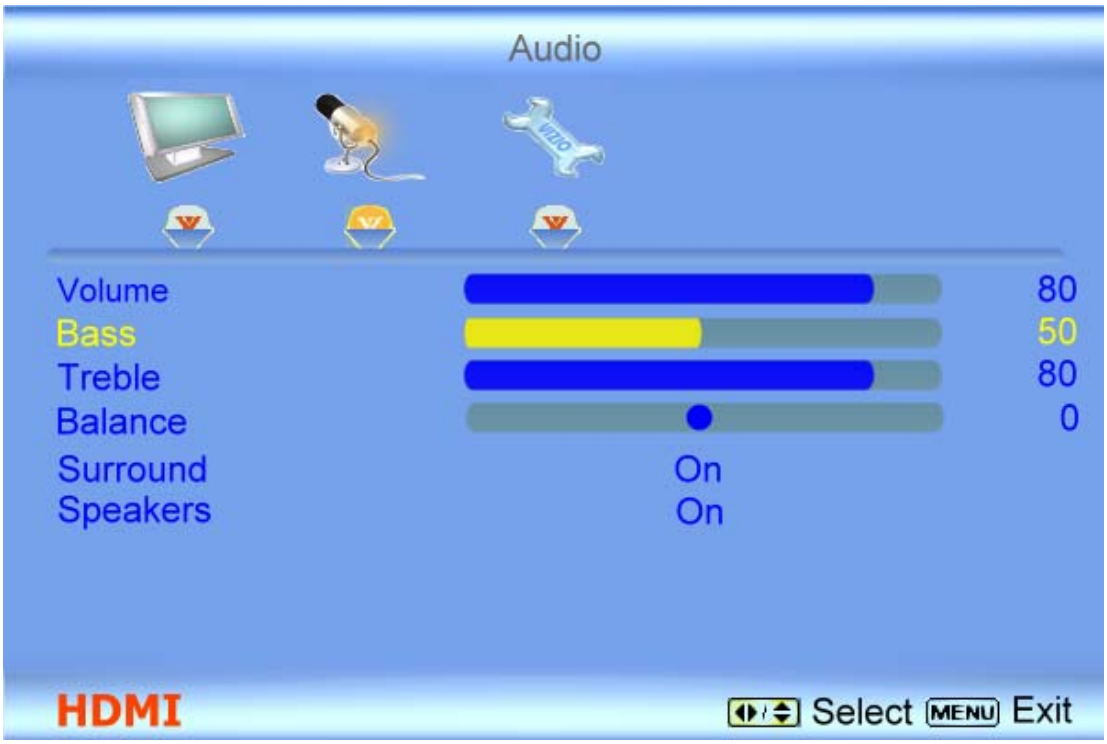
e. Tint (hue) (-32~32, **0**)

f. Sharpness (0~7, **4**)

g. Color Temperature (**Cool**/Normal/Warm/Custom)

h. Advanced Video

B. **Audio**：(**Bold: Default**)



a. Volume (0~100, **25**)

b. Bass (0~100, **50**)

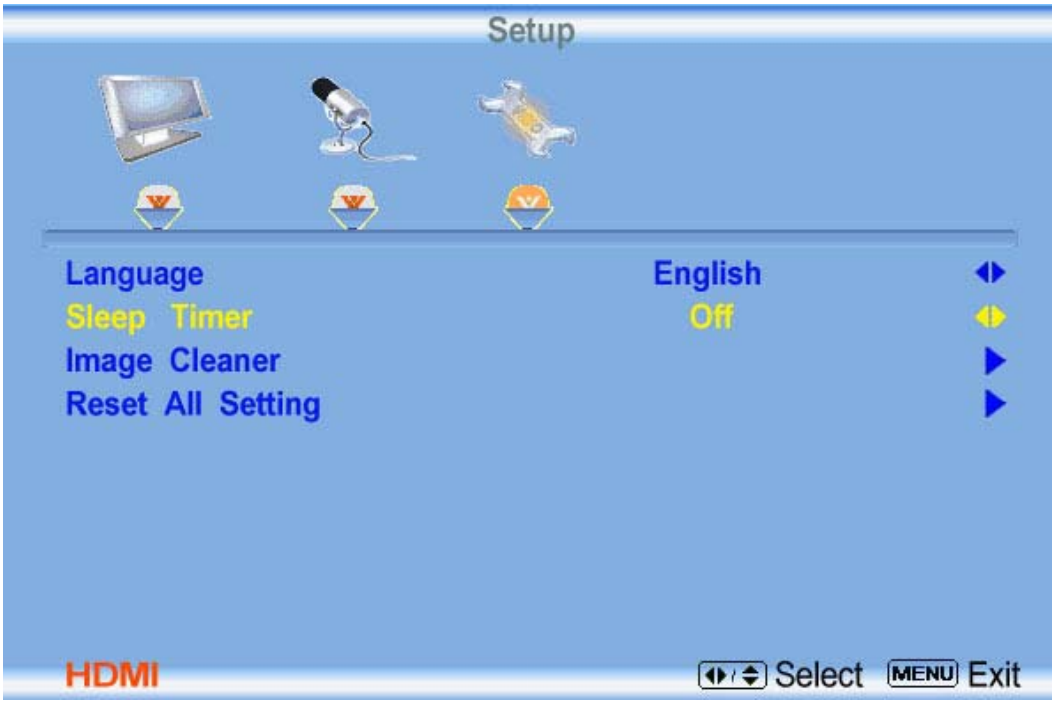
c. Treble (0~100, **50**)

d. Balance (-50~50, **0**)

e. Surround (**ON**/OFF)

f. Speakers (**ON**/OFF)

C. **Setup**：(**Bold: Default**)



a. Language (**Englis**h/ Français / Espaňol)

b. Sleep Timer (**OFF**/30Min/60Min/90Min/120Min)

c. Analog CC (**OFF**/CC1~4/TT1~4)

d. Digital CC (**OFF**/CC1~4/Service1~6)

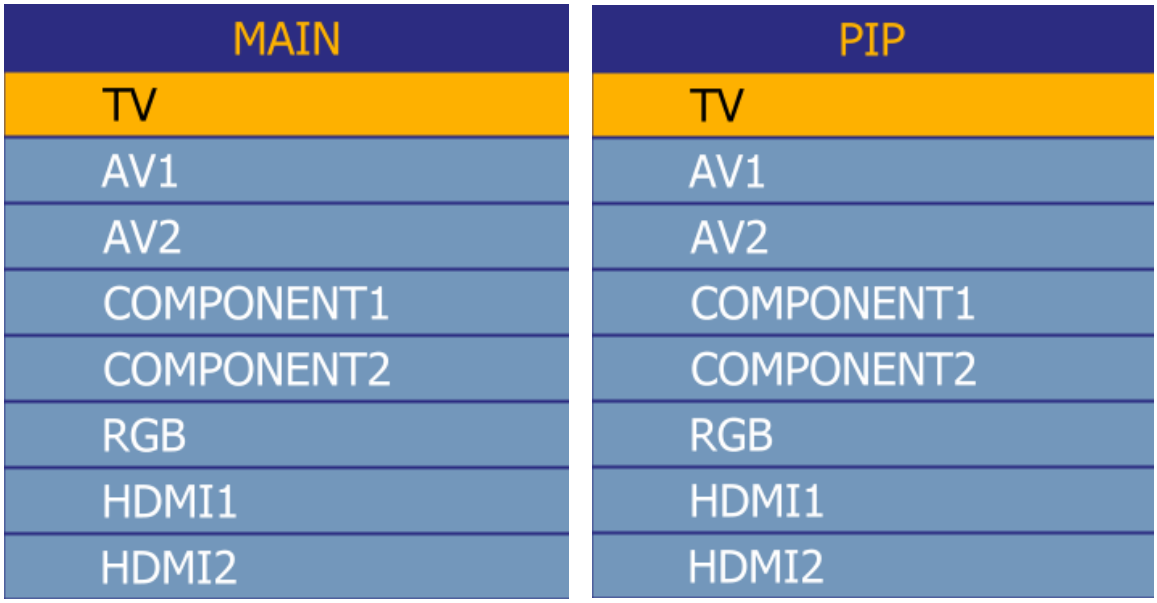
e. Digital CC Style

f. Image Cleaner (ON/**OFF**)

g. Rest All Setting (OK/**Cancel**)

[INPUT]

“INPUT” could supply an interface providing a list. The list shows input sources and provides the choices of different sources. The list includes items as below:



A. **TV**: Analog TV or digital TV

B. **AV1**, **AV2**: Composite (AV) signal

C. **Component1**, **Component2**: Color difference (YPbPr) video signals.

D. **RGB**: Video Graphics Array (VGA) or D-sub video signals.

E. **HDMI1**, **HDMI2**: High Definition Multimedia Interface (HDMI) multimedia signals.

***Note*：** The list of PIP provides the choices of different sources on sub-screen.

[INFO]

“INFO” button could show an information bar which displays the information about the input signal on our LCD TV.

Chapter4 Factory preset timings

This timing chart is already preset for the PDP analog & digital display monitors.

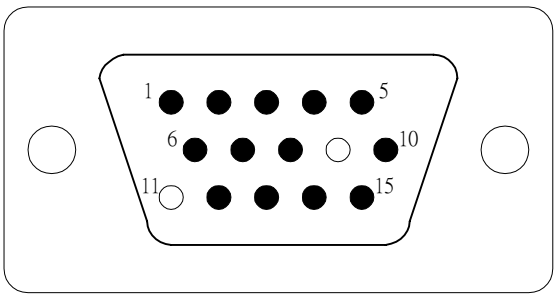
Resolution	Refresh rate	Horizontal Frequency	Vertical Frequency	Horizontal Polarity	Vertical Polarity	Pixel Rate
640x480	60Hz	31.5kHz	59.94Hz	N	N	25.175
640x480	75Hz	37.5kHz	75.00Hz	N	N	31.500
800X600	60Hz	37.9kHz	60.317Hz	P	P	40.000
800x600	75Hz	46.9kHz	75.00Hz	P	P	49.500
800X600	85Hz	53.7kHz	85.06Hz	P	P	56.250
1024x768	60Hz	48.4kHz	60.01Hz	N	N	65.000
1024X768	75Hz	60.0kHz	75.03Hz	P	P	78.750
720x400	70Hz	31.46kHz	70.08Hz	N	P	28.320
1366X768	60Hz	47.7KHZ	60.00HZ	P	N	85.500

Remark: P: positive N: negative

Chapter5 Pin Assignment

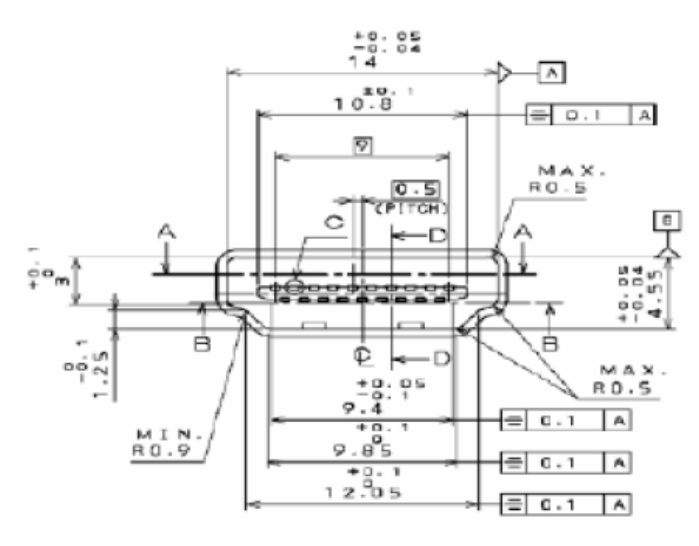
The TFT LCD analog display monitors use a 15 Pin Mini D-Sub connector as video input source.

Pin	Description
1	Red
2	Green
3	Blue
4	Ground
5	Ground
6	R-Ground
7	G-Ground
8	B-Ground
9	+5V for DDC
10	Ground
11	No Connection
12	(SDA)
13	H-Sync (Composite Sync)
14	V-Sync
15	(SCL)



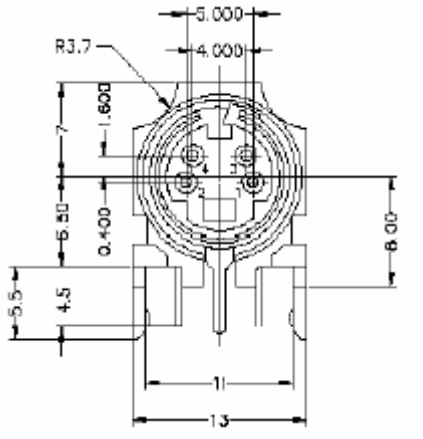
HDMI CONNECT PIN ASSIGNMENT

PIN	SIGNAL ASSIGNMENT
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2-
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1-
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0-
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	CEC
14	Reserved (N.C on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect



Four-Pin mini DIN S-Video Connector

a. Pin Assignment



b. Signal Level Video (Y): Analog 0.1Vp-p/75Ω

Video (C): Analog 0.286p-p/75

Sync (H+V): 0.3V below Video (Y)

c. Frequency H: 15.734KHz V: 60Hz (NTSC)

Signal Level Video (Y) : Analog 0.1Vp-p/75Ω

Video (C) : Analog 0.286p-p/75Ω

Sync (H+V): 0.3V below Video (Y)

Frequency H: 15.734Khz V: 60HZ (NTSC)

F-Type TV RF connector

a. Signal Level 60dBμV typical

b. System NTSC

c. Frequency 55~801MHz (NTSC)

PC connector 15 pin male D-sub connector

a. Pin Assignment Refer to Section 2.3.10

b. Signal Level Video (R, G, B): Analog 0.7Vp-p/75Ω

Sync (H, V): TTL level

RGB Signal:

a. Sync Type TTL (Separate / Composite) or Sync. On Green

b. Sync polarity Positive or Negative

c. Video Amplitude RGB: 0.7Vp-p

d. Frequency H: support to 30K~70KHz

V: support to 50~85Hz

Pixel Clock: support to 110MHz

HDMI Signal (HDMI):

a. Pin Assignment Refer to HDNI Pin Assignment

b. Type A

c. Polarity Positive or Negative

d. Frequency

H: 15.734KHz V: 60Hz (NTSC-480i)

H: 31KHz V: 60Hz (NTSC-480p)

H: 45KHz V: 60Hz (NTSC-720p)

H: 33KHz V: 60Hz (NTSC-1080i)

Component signal (Component 1 and Component 2)

Component 1

a. Frequency H: 15.734KHz V: 60Hz (NTSC-480i)
H: 31KHz V: 60Hz (NTSC-480p)
H: 45KHz V: 60Hz (NTSC-720p)
H: 33KHz V: 60Hz (NTSC-1080i)

b. Signal level Y: 1Vp-p Pb: ±0.350Vp-p Pr: ±0.350Vp-p

c. Impedance 75Ω

Component 2

a. Frequency H: 15.734KHz V: 60Hz (NTSC-480i)
H: 31KHz V: 60Hz (NTSC-480p)
H: 45KHz V: 60Hz (NTSC-720p)
H: 33KHz V: 60Hz (NTSC-1080i)

b. Signal level Y: 1Vp-p Pb: ±0.350Vp-p Pr: ±0.350Vp-p

c. Impedance 75Ω

Chapter6 Main Board I/o Connections

J9 CONNECTION [Main BD to Power BD and daughter BD]

Pin	Name	Description
1	“RLY_ON”	Control pin
2	“PWR_12V”	12V±5%
3	“12V_AUD”	11.84V±5%
4	“12V_AUD”	11.84V±5%
5	“GND”	“GND”
6	“GND”	“GND”
7	“GND”	“GND”
8	“GND”	“GND”
9	“5VSB”	5V±5%
10	“5VSC”	5V±5%
11	“5VSC”	5V±5%
12	“M5V_ON”	Control pin
13	“BL_ON/OFF”	Control pin
14	“AC_DEC”	Control pin

J1 CONNECTION [Main BD to daughter BD]

Pin	Name	Description
1	“PWR_12V”	12V±5%
2	“12V_AUD”	11.84V±5%
3	“12V_AUD”	11.84V±5%
4	“GND”	“GND”
5	“GND”	“GND”

J2 CONNECTION [Main BD to display BD]

Pin	Name	Description
1	“AMBER”	Control LED
2	“WHITE”	Non-use
3	“5VSB”	5V±5%
4	“5VSB”	5V±5%
5	OIRI	IR
6	“GND”	“GND”
7	“GND”	“GND”
8	“KEYPAD-ADC1”	“KEYPAD-ADC1”
9	“KEYPAD-ADC2”	“KEYPAD-ADC2”
10	“DV33SB”	3.3V±5%

J4 CONNECTOR [MAIN BD TO SIDE JACK]

Pin	Description
1	“AV1-IN”
2	“GND”
3	“AV1L-IN”
4	“GND”
5	“AV1R-IN”
6	“GND”
7	“SY1-IN”
8	“GND”
9	“SC1-IN”
10	“GND”
11	“SVDET1”
12	“NC”

J6 CONNECTOR [Main BD to Speaker]

Pin	Description
1	“R+”
2	“R-”
3	“L-”
4	“L+”

Chapter 7 Theory of Circuit Operation

The route of D-SUB 15pin input

An RGB (analog) signal is inputted the D-SUB 15pin to the *MT5372* which transfers it to a digital signal by the A/D converter. Then MT5372 generates a Low Voltage Differential Signal (LVDS) for display device.

The route of HDMI CON input

A HDMI (digital) signal is inputted the HDMI 1&2 CON to the *PI3HDMI412FT* switch. The passing signal is processed with the MT5372. Then MT5372 generates a LVDS for display device.

The route of HDTV & Component input

HDTV & Component signal is inputted to the MT5372. After processing, MT5372 generates a LVDS for display device. The audio signal is inputted *MT8291*. After processing, MT8291 transmits the signal to *TDA8946J*, an audio amplifier. Then, the amplified signal is the output audio signal.

The route of Video 1,2,3 & S-Video input

The Video 1,2 and S-Video signal is inputted to the MT5372.After processing, MT5372 generates a LVDS for display device. The audio signal is inputted MT8291. After processing, MT8291 transmits the signal to TDA8946J, an audio amplifier. Then, the amplified signal is the output audio signal.

The route of TV input

TV signal is demodulated by the tuner then the demodulating signal is divided into two parts, video and audio signal. The video signal is processed by MT5372 then MT5372 generates a LVDS for display device. The audio signal is transmitted in the route named SIF. The SIF signal is demodulated and decoded by MT5372. The decoded analog signal is transferred into I2S, which is digital signal, by MT5372. The I2S signal is inputted and transferred into analog signal by MT8291. After processing, MT8291 transmits the signal to TDA8946J, an audio amplifier. Then, the amplified signal is the output audio signal.

The route of DTV input

DTV signal demodulated by the tuner then the demodulating signal is divided into two parts, video and audio signal. The video signal is decoding by *MT5112*. The decoded signal, as the format of MPEG4, is transmitted to and processed by MT5372. Also, MT5372 generates a LVDS for display device. The audio signal is transmitted in the route named FAT-IN. The FAT-IN signal is demodulated and decoded by MT5372. The decoded analog signal is transferred into I2S, which is

digital signal, by MT5372. The I2S signal is inputted and transferred into analog signal by MT8291. After processing, MT8291 transmits the signal to TDA8946J, an audio amplifier. Then, the amplified signal is the output audio signal.

The operation of keypad

There are 7 keys to control and to select the function of VX37. Also, there is a LED back light under the logo “VIZIO” to indicate the status of operation (Orange => STANDBY, White => ON). They are “Power, ▼▲, + -, Input, MENU”.

MT5372

Ⅰ. GENERAL DESCRIPTION

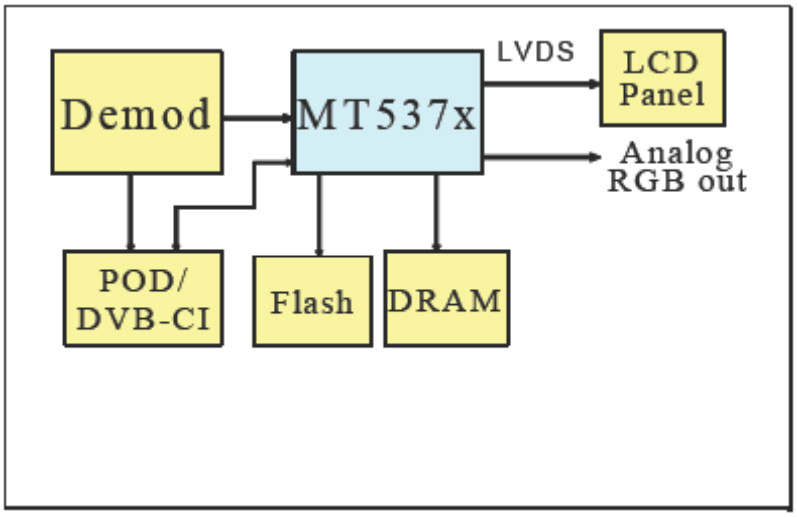
The **MediaTek MT5372** consists of a DTV backend decoder and a TV controller and offers high integration for advanced applications in main stream integrated digital television market. The MT5372 combines a transport de-multiplexer, a high definition MPEG-2 video decoder, an AC3 audio decoder, an LVDS transmitter, and an NTSC/PAL/SECAM video decoder with a 3D comb filter. The MT5372 enables consumer electronics manufactures to build high quality, feature-rich DTVs.

World-Leading Video Technology: The MT5372 includes MediaTek’s proprietary de-interlacing technology, the MDDiTM solution to generate very smooth picture quality for motions. A 3D comb filter added to the video decoder recovers great detail for still pictures. The special color processing technology provides natural colors and true studio quality graphics.

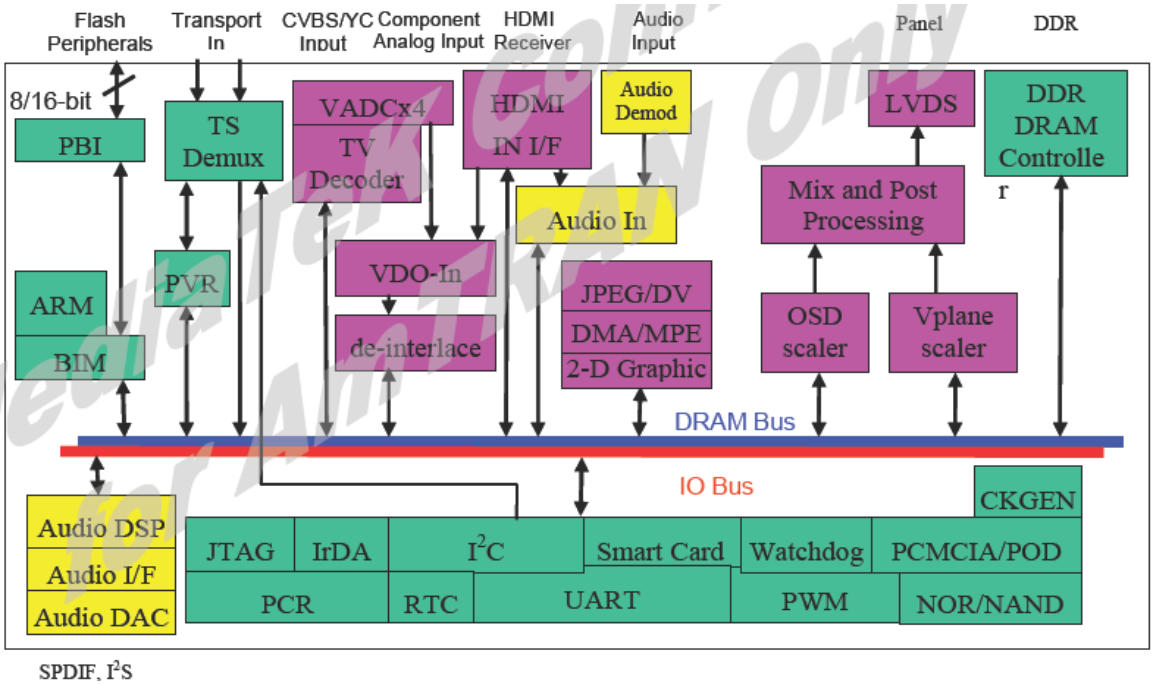
Rich Features for High Value Products: Additional features of iDTVs for the MT5372 release are the abilities to support the HDMI receiver, PIP/POP functionalities, memory cards and DV decoding.

Reliable Analog Technology: The MT5372 integrates high speed VGA ADC, high resolution Video/Audio ADC, 90db Audio DACs. The MT5372 provides very fine quality for the iDTV markets.

System Block Diagram



Functional Block Diagram



Ⅱ. Features of MT5372

1. Key Features:

1. A transport de-multiplexer
2. An MPEG-2 video decoder
3. An AC3 audio decoder
4. A 3D comb TV decoder
5. PIP/POP mode
6. An HDMI receiver
7. A set of three VGA ADCs

2. Host CPU:

1. ARM 926
2. 16K I-Cache and 16K D-Cache
3. 8K Data TCM and 8K Instruction TCM
4. JTAG ICE interface
5. Watch Dog timers
6. Built-in CPI analyzer

3. Transport De-multiplexer:

1. Supports one independent transport stream input
2. Supports serial / parallel interfaces for transport stream input
3. Supports ATSC, DVB, and MPEG2 transport stream inputs
4. Programmable sync detection
5. Supports DES/3-DES/DVB/Multi-2 de-scramblers
6. Up to 8 PIDs even/odd keys for descrambling
7. Supports 32 PID filters and 32 section filters
8. Supports positive/negative/mask section filtering

4. MPEG-2/JPEG Decoder:

1. Supports one MPEG-2 HD decoder
2. MPEG compliant with DV, MP@ML, MP@HL and MPEG-1 video standards
3. JPEG decode base-line or progressive JPEG file

5. 2D Graphics:

1. Supports multiple color modes
2. Point, horizontal/vertical line primitive drawings
3. Rectangle fill and gradient fill functions
4. Bitblt with transparent, alpha blending, alpha composition and stretch
5. Font rendering by color expansion
6. YCbCr to RGB color space transfer
7. Supports off-line scaler

6. OSD Plane:

1. Three linking list OSD with multiple color modes
2. Two OSD with scaler
3. Square size, 32x32 or 64x64 pixel, hardware cursor

7. Video Plane:

1. Supports clip
2. Flesh tone management
3. Gamma/anti-Gamma correction
4. Color Transient Improvement (CTI)
5. 2D peaking
6. Saturation/hue adjustment
7. Brightness and contrast adjustment
8. Black level extender
9. White peak level limiter
10. Adaptive Luma/Chroma management
11. Automatic detection of films or video sources
12. 3:2/2:2 pull down source detection
13. SD/HD advanced motion adaptive de-interlacing with excellent low angle
14. Arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X
15. Advanced linear and non-linear panoramic scaling.
16. Programmable zoom viewer
17. Progressive scan output
18. Supports alpha blending
19. Picture-in-Picture (PIP)
20. Picture-Outside-Picture (POP)
21. Dithering processing for flat panel display
22. Frame rate conversion, 50Hz to 75Hz
23. Supports mirror and upside down video outputs
24. Supports 480i/ 576i/ 480p /576p/ 720p/ 1080i/ 1080p output forma

8. LVDS:

1. One 10-bit channel or dual 6/8-bit channel
2. Built-in spread spectrum for EMI performance

3. Supports 6/8/10-bit format output
4. Programmable panel timing output

9. CVBS In:

1. On-chip 54MHz 10-bit video ADC
2. Supports PAL (B,G,D,H,M,N,I,Nc), PAL(Nc), PAL, NTSC, NTSC-4.43 and SECAM
3. Macrovision detection
4. NTSC/PAL support 3D Motion Adaptive comb filter and SECAM supports 2D comb filter
5. Built-in Motion Adaptive 3D Noise Reduction
6. VBI data slicer for CC/TT decoding
7. Supports four CVBS channels and two S-Video channels

10. CVBS Bypass:

1. Supports CVBS/S-Video bypass to Pin TP2
2. ATSC/DVB could not output to CVBS

11. VGA In:

1. Supports VGA input up to UXGA 150MHz
2. Supports full VESA standards

12. Component Video In:

1. Supports two component video inputs
2. Supports 480i/480p/576i/576p/720p/1080i/1080P, 1080P up to 60Hz

13. Digital Video-In Interface:

One 8-bit digital video-in interface for MT5372

14. Audio line In Interface:

1-bit data (two channel)

15. HDMI Receiver:

1. HDMI1.1
2. DVI 1.0
3. EIA/CEA-861B
4. HDCP 1.1
5. Supports up to 1080P 60Hz source

16. TV audio demodulator:

1. Supports BTSC/EIA-J/A2/NICAM/PAL, FM/SECAM world wild formats
2. Standard auto detection
3. Stereo demodulation, SAP demodulation
4. Noise reduction
5. Mode selection (Main/SAP/Stereo)
6. Pink noise and white noise generators
7. Equalizer
8. Sub-woofer/Bass enhancement
9. Noise auto mute
10. 3D surround processing include virtual surround
11. Audio and video lip synchronization
12. Supports reverberation

17. Audio DAC:

Four on-chip audio DACs support R/L channels and subwoofer outputs

18. DRAM Controller:

1. Supports 64Mb to 1Gb DDR DRAM devices
2. Configurable 16/32-bit data bus for MT5372
3. Supports DDR1-333, DDR1-400, DDR2-533, DDR2-667 JEDEC specification compliant SDRAM

19. Audio DSP:

1. Supports Dolby Digital AC-3 decoding (ATSC)
2. MPEG-1 layer I/II decoding (DVB)
3. MPEG-2 AAC decoding (Japan)
4. DV audio decoding
5. MP3 decoding
6. Dolby Pro-logic II
7. Audio output: 7.1ch + 2ch (down mix)
8. Pink noise and white noise generators
9. Equalizer
10. Bass management

11. 3D-surround processing with virtual surround
12. Audio and video lip synchronization
13. Supports reverberation
14. Automatic volume control
15. One SPDIF out
16. 5-bit data (10-channel) I2S out interface up to 24-bit resolution per channel

20. Peripherals:

1. Two UARTs with a transmitter and a receiver FIFO, one of them has a hardware flow control
2. Three serial interfaces, one is the master for general purposes, one is the master for the HDMI key, and the remaining one is the slave for the HDMI EDID data
4. Three PWMs
5. IR blaster and receiver
6. Real-time clock and watchdog controller
7. Smart Card reader
8. PCMCIA/POD/CI interfaces
9. Supports three NOR flash or one NOR and one NAND flash
10. Supports CableCARD host control bus

21. IC Outline:

1. The MT5372 is delivered in 588-ball BGA package
2. 3.3V/1.2V and 2.5V for DDR1; 1.8V for DDR2

Ⅲ. Electrical Characteristics

1. Absolute Maximum Rating

Symbol	Parameters	Value	Unit
IOVDD	3.3V supply voltage	-0.5 to 4.6	V
CVDD	1.2V supply voltage	-0.5 to 1.8	V
AVDD33	3.3V Analog supply voltage	-0.5 to 4.6	V
AVDD15	1.5V Analog supply voltage	-0.5 to 1.8	V
RVDD25	DDR1 supply voltage	-0.5 to 3.5	V
RVDD18	DDR2 supply voltage	-0.5 to 3.5	V
VIN(3.3V)	Input Voltage(3.3V IO)	VSS-1.0 to 3.63	V
VIN(5V tolerance)	Input Voltage(5V tolerance IO)	VSS-1.0 to 5.5	V
Vout	Output Voltage	-0.3 to VDD3+0.3	V
Ts	Storage Temperature	-40 to 150	C
Ta	Ambient Temperature	0 to 70	C

2. DC Characteristics

Symbol	Parameters	Min	Typical	Max	Unit
IOVDD	3.3V supply voltage	2.97	3.3	3.63	V
CVDD	1.2V supply voltage	1.08	1.2	1.32	V
AVDD	Analog supply voltage	2.97	3.3	3.63	V
VIH(3.3V)	3.3V input voltage high	2.0			V
VIL(3.3V)	3.3V input voltage low			0.8	V
VOH(3.3V)	3.3V output voltage high	2.4			
VOL(3.3V)	3.3V output voltage low			0.4	
VIH(3/5V)	3/5V tolerance input voltage high	2.0			V
VIL(3/5V)	3/5V tolerance input voltage low			0.8	V
VOH(3/5V)	3/5V tolerance output voltage high	2.4			V
VOL(3/5V)	3/5V tolerance output voltage low			0.4	V
Tj	Junction operation temperature	-40	25	125	C
PD(estimate)	Power dissapation		3		W
Pdown	Power down mode		2		mW

3. DDR1 ELECTRICAL Characteristics and DC Operating Condition

Symbol	Parameters	Min	Typical	Max	Unit
RVDD25(DDR333)	DDR I/O supply voltage for DDR266 or DDR333	2.3	2.5	2.7	V
RVDD25(DDR400)	DDR I/O supply voltage for DDR400	2.5	2.6	2.7	V
DVREF	DDR I/O reference voltage	0.49*RVDD	0.5*RVDD	0.51*RVDD	V
VTT	DDR I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V
VIH	DDR input voltage high	VREF+0.15		RVDD+0.3	V
VIL	DDR input voltage low	-0.3		VREF-0.15	V

4. DDR1 AC Operating Condition

Symbol	Parameters	Min	Typical	Max	Unit
VIH	Input high voltage, DQ, DQS	DVREF+0.31			V
VIL	Input low voltage, DQ, DQS			DVREF-0.31	V
Vslew	Input minimum slew rate	1.0			V/ns
Vswing	Input maximum swing			1.5	V

5. DDR2 ELECTRICAL Characteristics and DC Operating Condition

Symbol	Parameters	Min	Typical	Max	Unit
RVDD	DDR I/O supply voltage for DDR400	1.7	1.8	1.9	V
DVREF	DDR I/O reference voltage	0.49*RVDD	0.5*RVDD	0.51*RVDD	V
VTT	DDR I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V
VIH	DDR input voltage high	VREF+0.125		RVDD+0.3	V
VIL	DDR input voltage low	-0.3		VREF-0.125	V

6. DDR2 AC Operating Condition

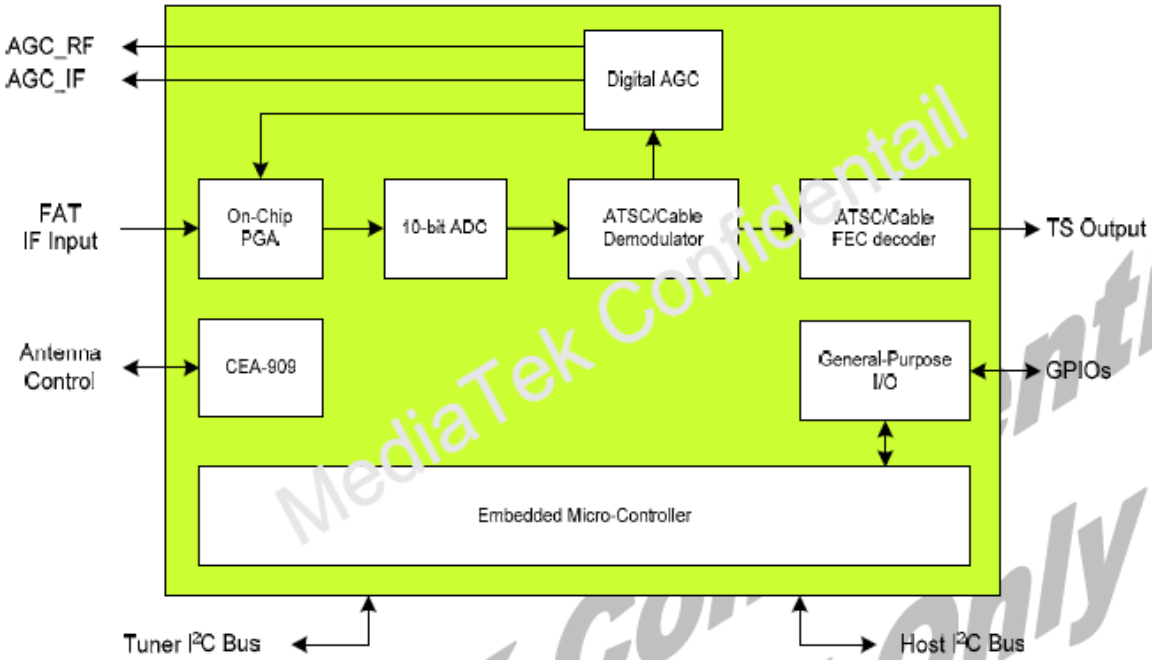
Symbol	Parameters	Min	Typical	Max	Unit
VIH(400, 533)	Input high voltage, DQ, DQS	DVREF+0.25			V
VIL(400, 533)	Input low voltage, DQ, DQS			DVREF-0.25	V
VIH(667, 800)	Input high voltage, DQ, DQS	DVREF+0.20			V
VIL(667, 800)	Input low voltage, DQ, DQS			DVREF-0.20	V
Vslew	Input minimum slew rate	1.0			V/ns
Vswing	Input maximum swing			1.0	V

MT5112

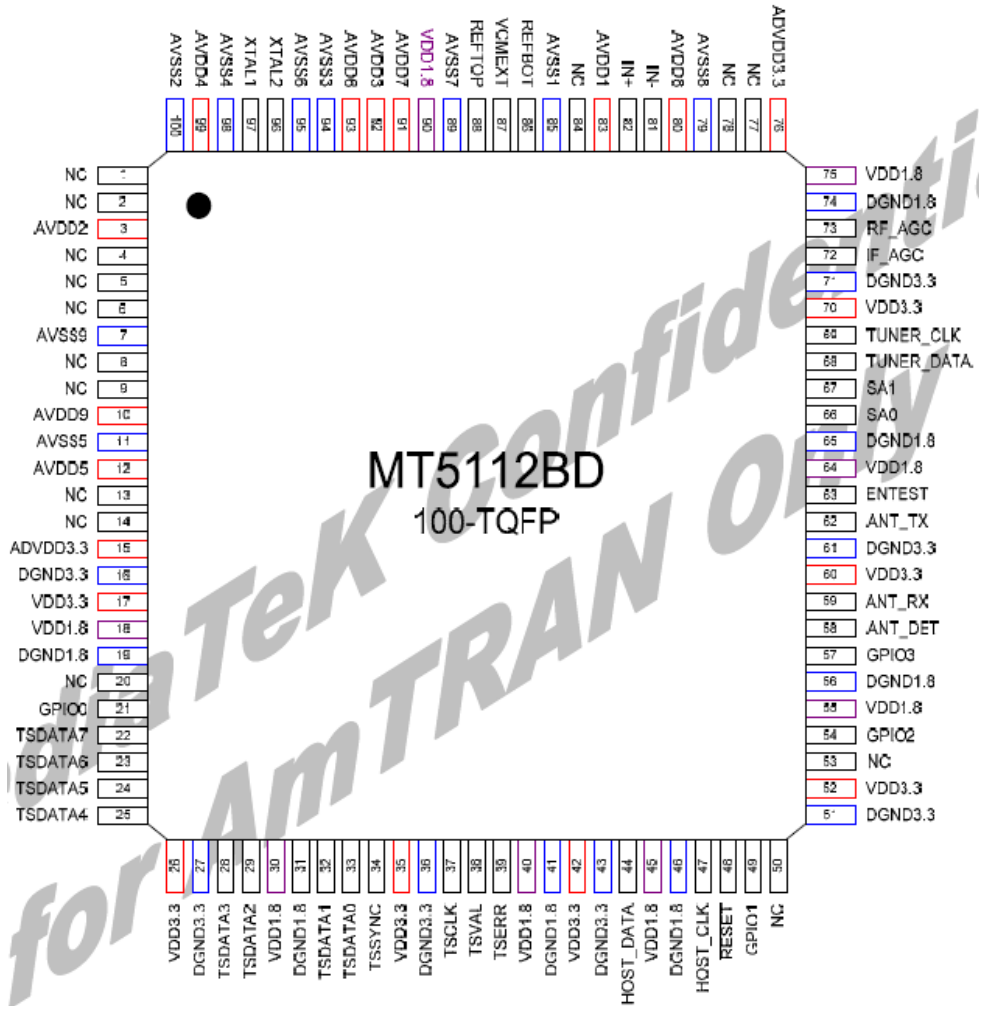
1. GENERAL DESCRIPTION

The MT5112BD is a highly integrated single-chip for digital terrestrial HDTV and digital cable TV de-modulation. The chip is designed specifically for the digital terrestrial HDTV and CATV receivers, and is fully compliant with ATSC A/53, SCTE DVS-031, and ITU J.83 Annex B standards.

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTION

For FAT Applications

Pin Numbers	Symbol	Type	Description
Transport Stream			
22, 23, 24, 25, 28, 29, 32, 33	TSDATA[7:0]	O	TS data output
34	TSSYNC	O	TS packet start signal
38	TSVAL	O	TS output valid signal
37	TSCLK	O	TS output clock
39	TSERR	O	TS packet error indicator
Analog Signal			
82	IN+	I	Analog differential IF input
81	IN-	I	
88	REFTOP	O	ADC reference top voltage. Decouple with a capacitor to AVSS
86	REFBOT	O	ADC reference bottom voltage. Decouple with a capacitor to AVSS
87	VCMEXT	O	ADC common mode voltage
Antenna Interface			
62	ANT_TX	O	CEA-909 antenna control: transmit data
58	ANT_DET	I	CEA-909 antenna control: detection signal
59	ANT_RX	I	CEA-909 antenna control: receive data
Clock Generation			
97	XTAL1	I	25MHz crystal input
96	XTAL2	I	
Clock Generation			
97	XTAL1	I	25MHz crystal input
96	XTAL2	I	
Control Signals			
47	HOST_CLK	I	Host processor serial clock input, 5 volt compatible
44	HOST_DATA	I/O	Host processor serial data pin, 5 volt compatible
69	TUNER_CLK	O	Tuner serial clock output, 5 volt compatible
68	TUNER_DATA	I/O	Tuner serial data pin, 5 volt compatible
72	IF_AGC	O	IF AGC output
73	RF_AGC	O	RF AGC output
48	RESET	I	Power reset pin, low active
66	SA0	I	Chip slave address selection pin, tie to VDD3.3 or DGND
67	SA1	I	Chip slave address selection pin, tie to VDD3.3 or DGND
Power Supply			
17, 26, 35, 42, 52, 60, 70	VDD3.3	P	Digital power supply, tie to 3.3V
18, 30, 40, 45, 55, 64, 75	VDD1.8	P	Digital power supply, tie to 1.8V
16, 19, 27, 31, 36, 41, 43, 46, 51, 56, 61, 63, 65, 71, 74	DGND	P	Digital ground, tie to digital ground plane
3, 10, 12, 80, 83, 91, 92, 93, 99	AVDD	P	Analog power supply, tie to 3.3V
7, 11, 79, 85, 89, 94, 95, 98, 100	AVSS	P	Analog ground, tie to analog ground plane
15, 76	ADVDD3.3	P	Digital power supply for analog component, tie to 3.3V
90	AVDD1.8	P	Digital power supply for analog component, tie to 1.8V
General-Purpose I/O			
57, 54, 49, 21	GPIO[3:0]	I/O	General-Purpose I/Os

2. 8-VSB and Clear-QAM Reception

MT5112BD contains a 10-bit A/D converter, an 8-VSB/QAM demodulator, followed by a trellis-code de-modulation (TCM) decoder and a Reed-Solomon forward error correction (FEC) decoder. Moreover, an embedded 8-bit microprocessor intelligently handles the acquisition and tracking to ensure the best receiving performance under various channel conditions. The microprocessor communicates with the external host controller via an I2C-compatible interface, and also provides direct control to the RF tuner via another I2C-compatible interface.

MT5112BD accepts the tuner IF output centered at 44MHz or 43.75MHz, or the low IF signals from a down-converter. With good adjacent channel immunity, additional IF SAW filters for adjacent channel rejection can be saved. An on-chip programmable gain-controlled amplifier (PGA) is designed to provide extra signal gain when the tuner output level is low. The amplified IF signal is then sample and digitized for further demodulation process.

MT5112BD keeps A/D input power level at a desired level so as to maximize the received SNR. It measures the power level of the digitized samples and provide two signals (both sigma-delta encoded; one delayed and one non-delayed) for front-end gain control purpose. The signals is low-pass filtered before connected to tuner or IF gain stages.

For the 8-VSB reception, the carrier frequency offset is estimated and compensated by a fully digital synchronizer. It also controls the rate conversion in the digital re-sampling device by estimating the sampling frequency offset; hence no external VCXO is required. The digital synchronizer simultaneously offers very wide frequency acquisition range and stable tracking capability. This makes MT5112BD robust work under severe impairment conditions.

The MT5112BD is equipped with a powerful equalizer for mitigating the multi-path effects due to terrestrial propagation of 8-VSB signals. The delicate equalizer design makes the MT5112BD boast its ability for strong echo cancellation. With this powerful equalizer, the MT5112BD can not only easily pass the tests of A74 equalization mask, ATTC channel ensembles, CRC channel ensembles, but also provide superior capability of live signal receptions.

For cable signal reception, the MT5112BD adopts the fully digital modules for timing and carrier synchronization, with no external VCXO required. Specially designed carrier synchronization module enables the MT5112BD passing the OpenCable ATP burst and phase noise tests, while maintaining excellent reception performance under normal reception conditions.

The MT5112BD also utilizes a powerful equalizer for performing channel equalization in cable environments. The MT5112BD equipped with this powerful equalizer can easily pass the SCTE channel tests and offer stable and excellent live signal receptions.

The following FEC decoder corrects most of the errors by the concatenation of the TCM and Reed-Solomon decoders with an in-between de-interleaver. Specifically for the digital cable TV reception, the MT5112BD first detects and aligns de-puncturing timing of the received sequence before TCM decoding. Besides, two synchronization circuits are each inserted before the de-interleaver and after the Reed-Solomon decoder to automatically delineate the FEC frames and transport stream packets respectively. An on-chip error rate estimator can simultaneously monitor the receiving qualities at the three stages: the equalizer output, the TCM decoder, and the transport stream packets. At the last stage, the MT5112BD incorporates a buffer to smooth out the uneven arrival time of transport stream packets. The chip finally outputs the smoothed decoded MPEG-2 transport stream packets in either the serial or parallel transport stream format.

In addition to the demodulation of HDTV signal, MT5112BD provides the capability to remove narrow-band interference such as the co-channel NTSC signal and CW tones which generally exists in broadcast environment.
To achieve the best reception, an antenna control interface compliant with EIA/CEA-909 is equipped into the MT5112BD to configure the antenna parameters. Both the unidirectional mode A and the bi-directional mode B operation schemes are supported.

3. FEATURES

1. Compliant with ATSC digital television standard
2. Supports SCTE DVS-031 and ITU J.83 Annex B digital CATV standard
3. Accepts direct IF (44 MHz or 43.75MHz) and low IF (5.38MHz)
4. Differential IF input with programmable input signal level: 0.5Vpp to 2Vpp
5. NTSC interference rejection capability
6. Compensate echo up to -35 to +60*us* range for terrestrial HDTV reception
7. Pass all Brazil fading channel ensembles
8. Meet all ATSC/A74 requirements.
9. On-chip programmable gain amplifier

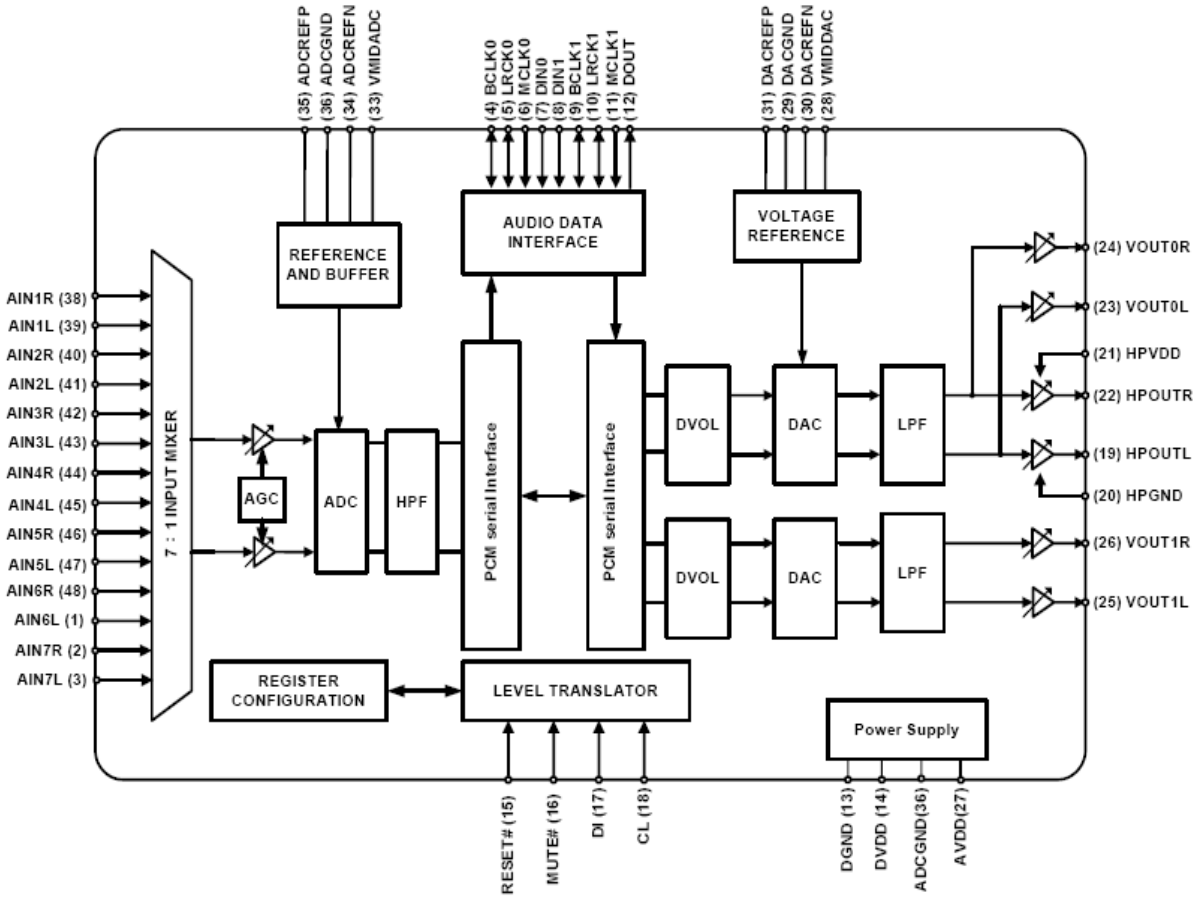
10. 25MHz crystal for clock generation
11. Excellent adjacent and co-channel rejection capability, only single SAW is required

12. Full-digital timing recovery, no VCXO is required
13. Full-digital frequency offset recovery with wide acquisition range ±1MHz for ATSC and ±250kHz for CATV reception
14. Dual digital AGC controls for IF and RF respectively
15. MPEG-2 transport stream output in parallel or serial format
16. On-chip error rate estimators for TS packets, TCM decoder, and equalizer
17. EIA/CEA-909 antenna interface, both mode A and mode B are supported
18. Controlled by I2C interface
19. Supports sleep mode to save power consumption
20. Core power supply: 1.8V, peripheral power supply: 3.3V
21. 100-TQFP with lead free package

MT8291

The **MediaTek MT8291** is a highly integrated stereo audio CODEC. The MT8291 performs stereo analog-to-digital and two digital-to-analog conversions with single-ended analog voltage input and output. It's up to 24-bit serial values at sample rates up to 192 kHz. A 7:1 stereo input multiplexer and an automatic level control are included. The PGA is available for line inputs and provides gain/attenuation of 21dB in 0.5 steps.
Two DAC outputs reach 2Vrms in a 12V supply environment including a headphone, two left/right line outputs with volume gain/attenuation from -127 dB to +12 dB and digital de-emphasis function. Sampled data is transmitted through the serial audio interface at various rates from 32 kHz to 192 kHz. For audio clock applications, the MT8291 supports master, slave modes and three data formats in the serial interface. Two individual sets of I2S ports including three clocks and digital data for each simultaneously support different sample rates for the ADC and DACs and then output from DAC1 and DAC2 independently.

1. BLOCK DIAGRAM



2. Key Feather

- 48-pin LQFP package
- 2 Vrms DAC output
- MUTE and RESET functions
- 7-channel input multiplexer with ADC programmable gain amplifier's (PGA's) gain from +21dB to –21dB in 0.5dB step
- Two individual sets of I2S ports simultaneously support different sample rates for the ADC and DACs and then output from DAC1 and DAC2 independently

3. Feather List

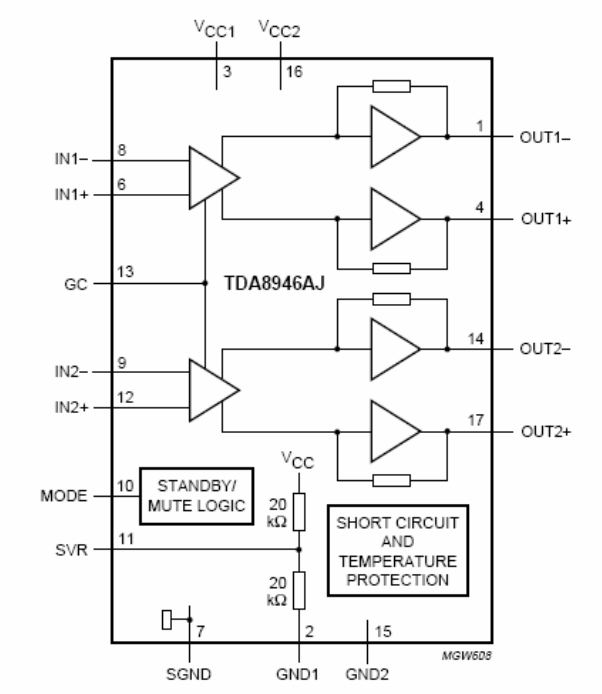
- 24-bit Sigma- Delta ADC and DAC
- Allows 2Vrms input swing into ADC part
- ADC up to 96 kHz sampling rates
- 90 dB ADC dynamic range
- Automatic gain control (AGC)
- 90 dB DAC dynamic range
- DAC up to 192 kHz sampling rates
- Two channels of ADC and four independent channels of DACs (two L/R line outputs and a headphone output)
- Supports two sets of I^2S clocks and data inputs independently
- System clocks: 128Fs, 192Fs, 256Fs, 384Fs, 512Fs, 768Fs
- Selectable serial audio interface formats:

  Left justified, right justified and I^2S up to 24 bits
- +3.0V to +3.6V digital power supply
- +8.2V to +13.2V analog power supply

TDA8946

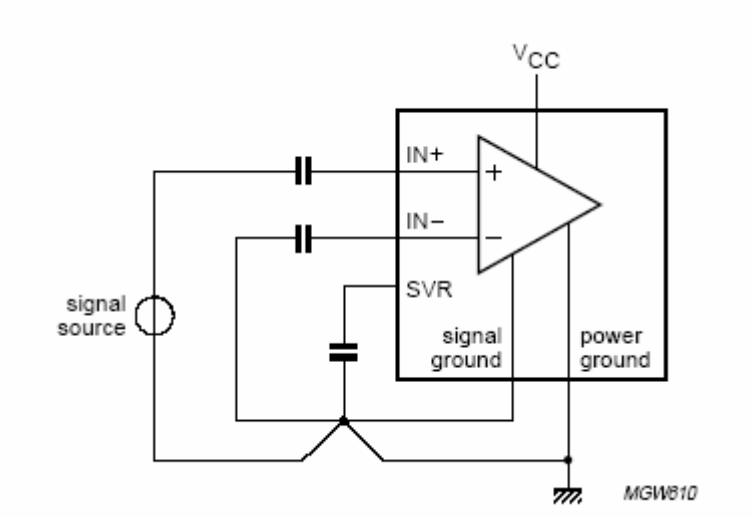
In L32 TV the TDA8946AJ is a dual-channel audio power amplifier with DC gain control. It has an output power of 2 . 10 W at an 8 . load and a 12 V supply.

Block diagram


VCC1
VCC2
3
16
1
OUT1−
IN1−
8
IN1+
6
4
OUT1+
GC
13
TDA8946AJ
14
OUT2−
IN2−
9
IN2+
12
17
OUT2+
VCC
MODE
10
STANDBY/
MUTE LOGIC
20
kΩ
SHORT CIRCUIT
AND
TEMPERATURE
PROTECTION
SVR
11
20
kΩ
7
2
15
MGW608
SGND
GND1
GND2

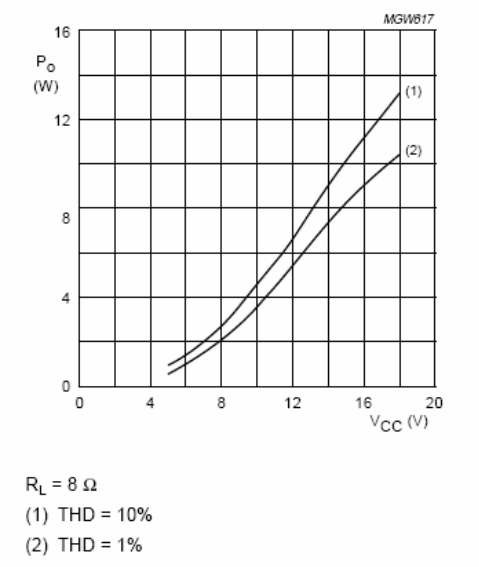
1. Input configuration

The TDA8946AJ inputs can be driven symmetrical (floating) as well as asymmetrical. In the asymmetrical mode one input pin is connected via a capacitor to the signal source and the other input is connected to the signal ground. The signal ground should be as close as possible to the SVR (electrolytic) capacitor ground. Note that the DC level of the input pins is half of the supply voltage VCC, so coupling capacitors for both pins are necessary



2. Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10%,in the L32 LCD TV Vcc=12V so we can see as shown in the following figure output about 7W.



R_L = 8 Ω
(1) THD = 10%
(2) THD = 1%

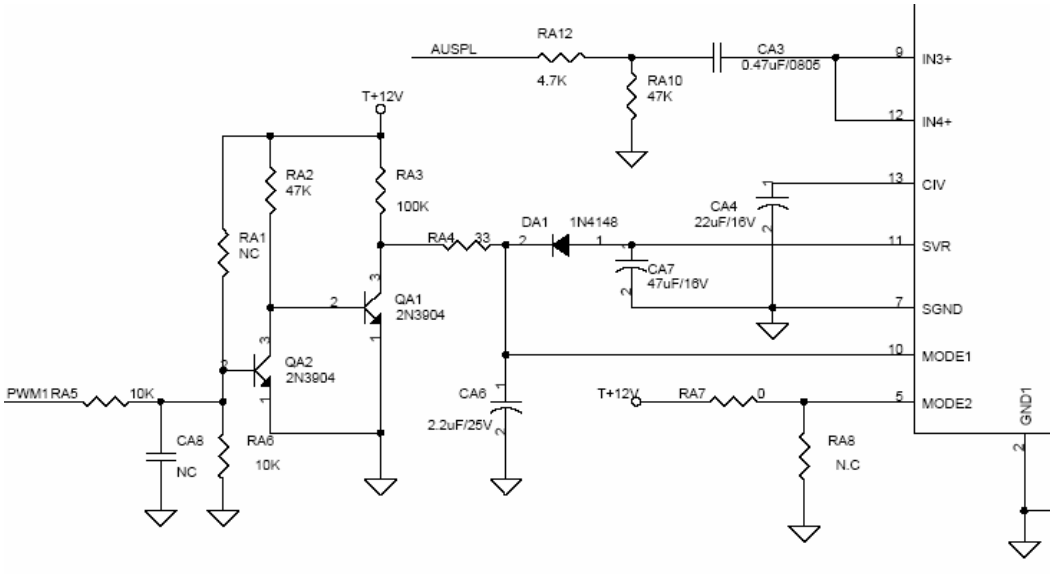
---

3. Mode selection

In the L32 LCD TV TDA8946AJ has two functional modes, which can be selected by applying the proper DC voltage to pin MODE.

1. Mute — In this mode the amplifier is DC-biased but not operational (no audio output). This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when 3.5 V < VMODE < (VCC − 1.5 V).

2. Operating — In this mode the amplifier is operating normally. The operating mode is activated at VMODE<1.0V.



The MX29LV320AT/B is a 32-mega bit Flash memory organized as 4M bytes of 8 bits and 2M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory.

The MX29LV320AT/B is packaged in 48-pin TSOP and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers. The standard MX29LV320AT/B offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV320AT/B has separate chip enable (CE) and output enable (OE) controls.

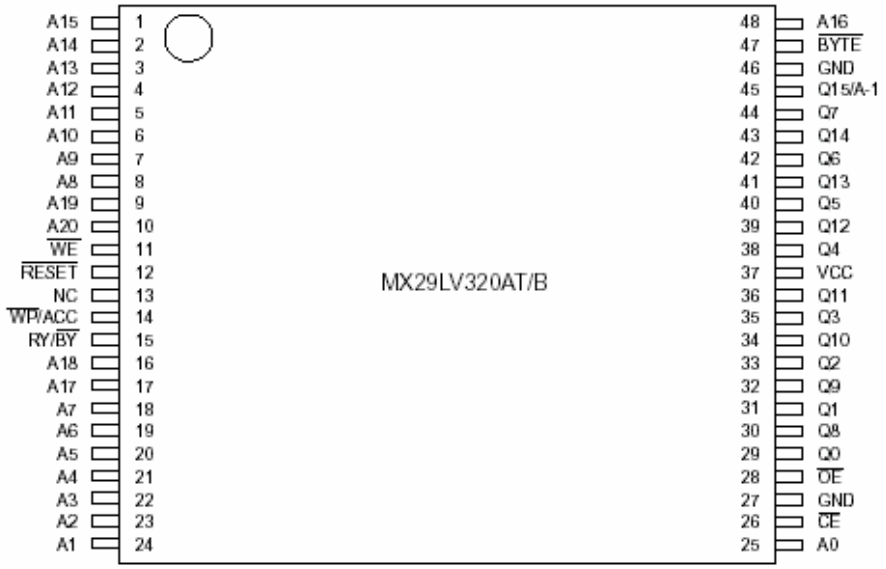
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV320AT/B uses a command register to manage this functionality. MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling.

The MX29LV320AT/B uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATION

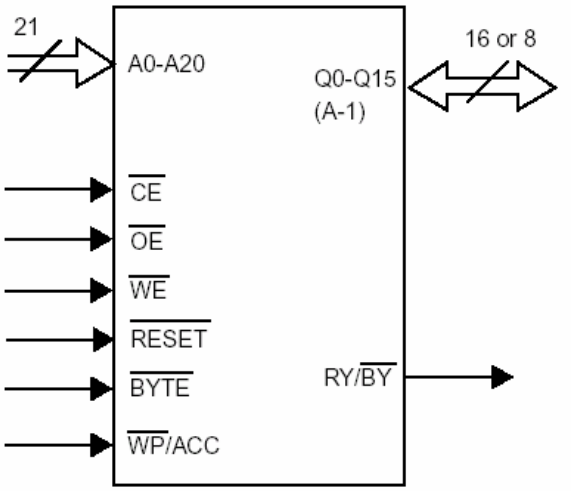
48 TSOP



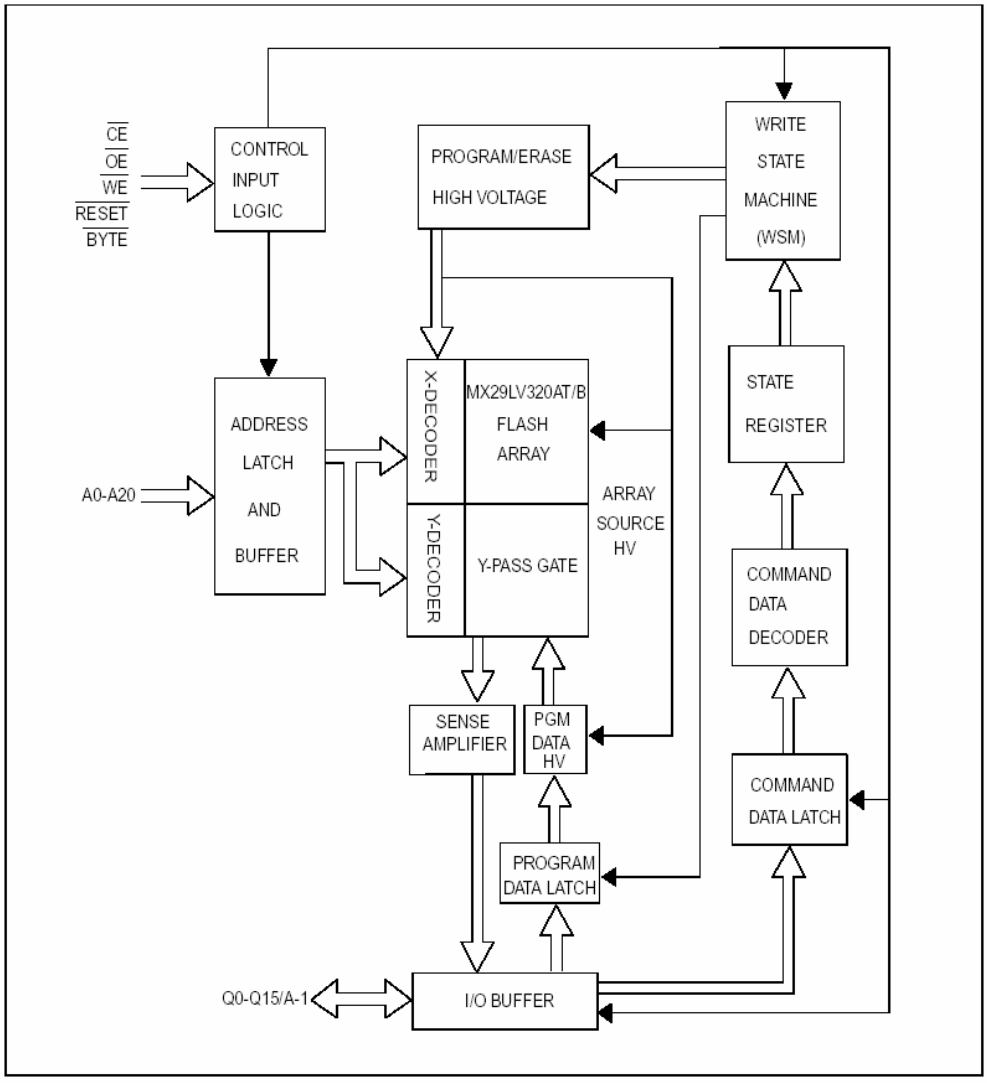
PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q14	15 Data Inputs/Outputs
Q15/A-1	Q15(Data Input/Output, word mode) A-1(LSB Address Input, byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$	Word/Byte Selection Input
$\overline{RESET}$	Hardware Reset Pin, Active Low
RY/$\overline{BY}$	Read/Busy Output
VCC	3.0 volt-only single power supply
$\overline{WP}$/ACC	Hardware Write Protect/Acceleration Pin
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



BLOCK DIAGRAM



BUS OPERATION--1

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	$\overline{WP}$/ACC	Addresses (Note 2)	Q0~Q7	Q8 ~ Q15	
								$\overline{Byte}$=VIH	$\overline{Byte}$=VIL
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	Q8-A14 =High-Z Q15=A-1
Write (Note 1)	L	H	L	H	Note 3	A_{IN}	D_{IN}	D_{IN}	
Accelerate Program	L	H	L	H	V_{HH}	A_{IN}	D_{IN}	D_{IN}	
Standby	VCC ± 0.3V	X	X	VCC ± 0.3V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	L/H	Sector Addresses, A6=L, A1=H, A0=L	D_{IN}, D_{OUT}	X	X
Chip Unprotect (Note 2)	L	H	L	V_{ID}	Note 3	Sector Addresses, A6=H, A1=H, A0=L	D_{IN}, D_{OUT}	X	X
Temporary Sector Group Unprotect	X	X	X	V_{ID}	Note 3	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend:

L=Logic LOW=VIL, H=Logic High=VIH, VID=12.0 0.5V, VHH=11.5-12.5V, X=Don't Care, AIN=Address IN, DIN=Data IN,DOUT=Data OUT

Notes:

1. When the WP/ACC pin is at VHH, the device enters the accelerated program mode. See "Accelerated Program Operations" for more information.
2. The sector group protect and chip unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Chip Unprotection" section.
3. If WP/ACC=VIL, the two outermost boot sectors remain protected. If WP/ACC=VIH, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP/ACC=VHH, all sectors will be unprotected.
4. DIN or Dout as required by command sequence, data polling, or sector protection algorithm.
5. Address are A20:A0 in word mode (BYTE=VIH), A20:A-1 in byte mode (BYTE=VIL).

BUS OPERATION--2

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A20 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q0-Q7	Q8-Q15
Read Silicon ID Manufacturer Code	L	L	H	X	X	V_{ID}	X	L	X	L	L	C2H	X
Read Silicon ID MX29LV320AT	L	L	H	X	X	V_{ID}	X	L	X	L	H	A7H	22h(word)
													X (byte)
Read Silicon ID MX29LV320AB	L	L	H	X	X	V_{ID}	X	L	X	L	H	A8H	22h(word)
													X (byte)
Sector Protect Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h(1), or 00h	X
Security Sector Indicater Bit (Q7)	L	L	H	X	X	V_{ID}	X	L	X	H	H	99h(2), or 19h	X

Notes:

1.Code=00h means unprotected, or code=01h protected.

2.Code=99 means factory locked, or code=19h not factory locked.

WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory , the system must drive WE and CE to VIL, and OE to VIH.An erase operation can erase one sector, multiple sectors , or the entire device. A "sector address" consists of the address bits required to uniquely select a sector. Writing specific address and data commands or sequences into the command register initiates device operations. Table A defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the Automatic Select command sequence, the device enters the Automatic Select mode. The system can then read Automatic Select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Automatic Select Mode and Automatic Select Command Sequence section for more information.ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

TABLE A. MX29LV320AT/B COMMAND DEFINITIONS

Command		Bus	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Cycles	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read(Note 5)		1	RA	RD										
Reset(Note 4)		1	XXX	F0										
Automatic Select(Note 5)														
Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	C2H				
	Byte	4	AAA	AA	555	55	AAA	90	X00	C2H				
Device ID	Word	4	555	AA	2AA	55	555	90	X01	ID				
	Byte	4	AAA	AA	555	55	AAA	90	X02					
Security Sector Factory	Word	4	555	AA	2AA	55	555	90	X03	99/19				
Protect Verify (Note 6)	Byte	4	AAA	AA	555	55	AAA	90	X06					
Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
(Note 7)	Byte	4	AAA	AA	555	55	AAA	90	(SA)X04					
Enter Security Sector	Word	3	555	AA	2AA	55	555	88						
Region	Byte	3	AAA	AA	555	55	AAA	88						
Exit Security Sector	Word	4	555	AA	2AA	55	555	90	XXX	00				
	Byte	4	AAA	AA	555	55	AAA	90	XXX	00				
Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte	4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
CFI Query (Note 8)	Word	1	55	98										
	Byte	1	AA	98										
Erase Suspend(Note 9)		1	SA	B0										
Erase Resume(Note 10)		1	SA	30										

Legend:
X=Don't care
RA=Address of the memory location to be read.
RD=Data read from location RA during read operation.
PA=Address of the memory location to be programmed.
Addresses are latched on the falling edge of the WE or CE pulse.
PD=Data to be programmed at location PA. Data is latched on the rising edge of WE or CE pulse.
SA=Address of the sector to be erased or verified. Address bits A20-A12 uniquely select any sector.
ID=22A7h(Top), 22A8h(Bottom)

Notes:

1.All values are in hexadecimal.
2.Except when reading array or Automatic Select data, all bus cycles are write operation.
3.The Reset command is required to return to the read mode when the device is in the Automatic Select mode or if Q5 goes high.
4.The fourth cycle of the Automatic Select command sequence is a read cycle.
5.The data is 99h for factory locked and 19h for not factory locked.
6.The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block. In the third cycle of the command sequence, address bit A20=0 to verify sectors 0~31, A20=1 to verify sectors 32~70 for Top Boot device.
7.Command is valid when device is ready to read array data or when device is in Automatic Select mode.
8.The system may read and program functions in non-erasing sectors, or enter the Automatic Select mode, when in the erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
9.The Erase Resume command is valid only during the Erase Suspend mode.

STANDBY MODE

MX29LV320AT/B can be set into Standby mode with two different approaches. One is using both CE and RESET pins and the other one is using RESET pin only.

When using both pins of CE and RESET, a CMOS Standby mode is achieved with both pins held at Vcc ±0.3V. Under this condition, the current consumed is less than 0.2uA (typ.). If both of the CE and RESET are held at VIH, but not within the range of VCC ± 0.3V, the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, Vcc active current (ICC2) is required even CE = "H" until the operation is completed. The device can be read with standard access time (tCE) from either of these standby modes.

When using only RESET, a CMOS standby mode is achieved with RESET input held at Vss ± 0.3V, Under this condition the current is consumed less than 1uA (typ.). Once the RESET pin is taken high, the device is back to active without recovery delay.In the standby mode the outputs are in the high impedance state, independent of the OE input.MX29LV320AT/B is capable to provide the Automatic Standby Mode to restrain power consumption during readout of data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To active this mode, MX29LV320AT/B automatically switch themselves to low power mode when MX29LV320AT/B addresses remain stable during access time of tACC+30ns. It is not necessary to control CE, WE, and OE on the mode. Under the mode, the current consumed is typically 0.2uA (CMOS level).

RESET OPERATION

01The RESET pin provides a hardware method of resetting the device to reading array data. When the RESET pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET pulse. When RESET is held at VSS 0.3V, the device draws CMOS standby current (ICC4). If RESET is held at VIL but not within VSS 0.3V, the standby current will be greater.The RESET pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firm-ware from the Flash memory.

If RESET is asserted during a program or erase operation, the RY/BY pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The system can thus monitor RY/BY to determine whether the reset operation is complete. If RESET is asserted when a program or erase operation is not executing (RY/BY pin is "1"), the reset operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the RESET pin returns to VIH. Refer to the AC Characteristics tables for RESET parameters and to Figure 14 for the timing diagram.

WRITE PROTECT (WP)

The write protect function provides a hardware method to protect boot sectors without using VID.

If the system asserts VIL on the WP/ACC pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in Sector/Sector Group Protection and Chip Unprotection". The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts VIH on the WP/ACC pin, the device reverts to whether the two outermost 8K Byte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last

protected or unprotected using the method described in "Sector/Sector Group Protection and Chip Unprotection".
Note that the WP/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

SOFTWARE COMMAND DEFINITIONS :

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device (whenapplicable).

All addresses are latched on the falling edge of WE or CE, whichever happens later. All data are latched on rising edge of WE or CE, whichever happens first.

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY.Table B and the following subsections describe the functions of these bits. Q7, RY/BY, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Table B. Write Operation Status

	Status		Q7 Note1	Q6	Q5 Note2	Q3	Q2	RY/$\overline{BY}$
In Progress	Byte/Word Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	1
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	1
		Erase Suspend Program	$\overline{Q7}$	Toggle	0	N/A	N/A	0
Exceeded Time Limits	Byte/Word Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	N/A	No Toggle	0
	Auto Erase Algorithm		0	Toggle	1	1	Toggle	0
	Erase Suspend Program		$\overline{Q7}$	Toggle	1	N/A	N/A	0

Notes:

1.Performing successive read operations from the erase-suspended sector will cause Q2 to toggle.

2.Performing successive read operations from any address will cause Q6 to toggle.

3.Reading the byte/word address being programmed while in the erase-suspend program

mode will indicate logic "1" at the Q2 bit.
However, successive reads from the erase-suspended sector will cause Q2 to toggle.

Fig C. COMMAND WRITE OPERATION

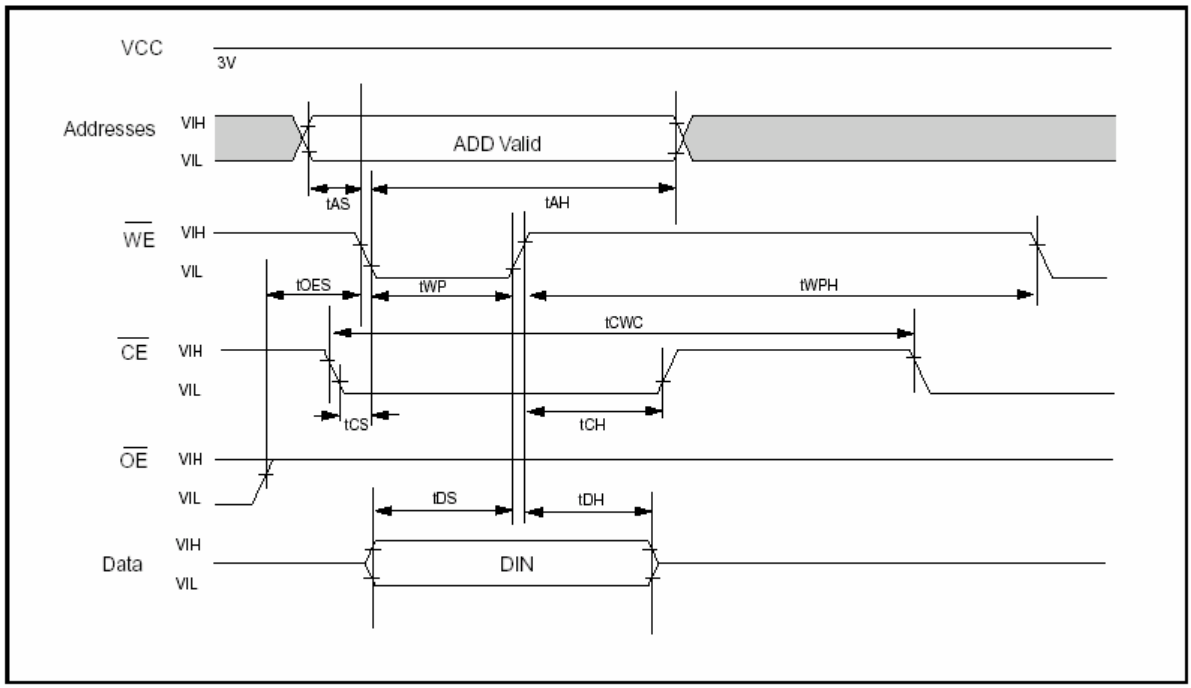
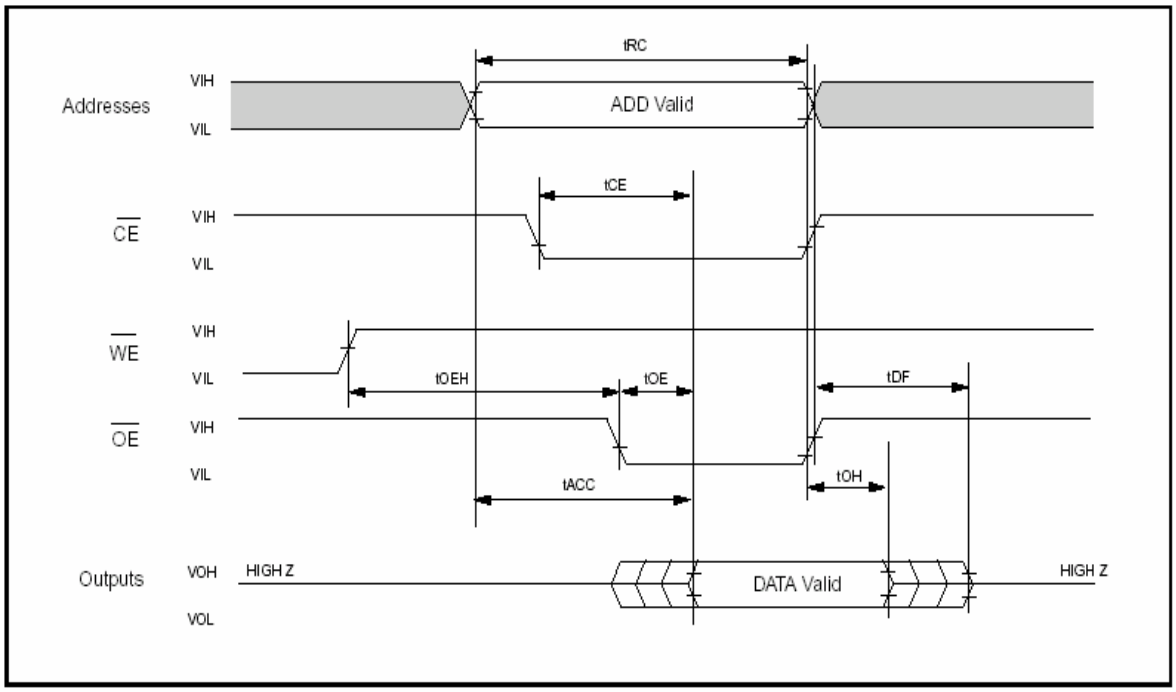


Fig D. READ TIMING WAVEFORMS

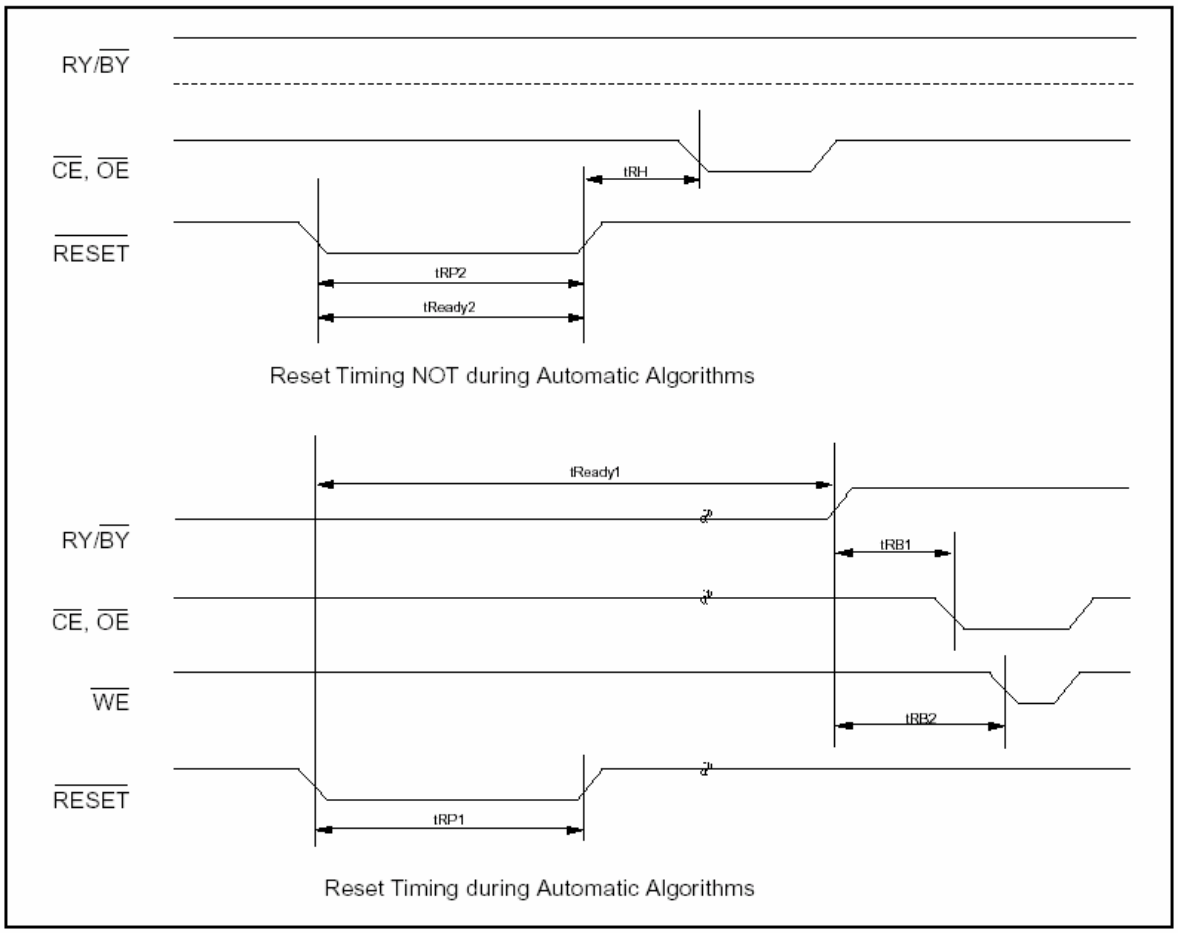

tRC
Addresses
VIH
VIL
ADD Valid
tCE
CE
VIH
VIL
WE
VIH
VIL
tOEH
tOE
tDF
OE
VIH
VIL
tOH
tACC
Outputs
VOH
VOL
HIGH Z
DATA Valid
HIGH Z

AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tREADY1	$\overline{\text{RESET}}$ PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	$\overline{\text{RESET}}$ PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP1	$\overline{\text{RESET}}$ Pulse Width (During Automatic Algorithms)	MIN	10	us
tRP2	$\overline{\text{RESET}}$ Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	$\overline{\text{RESET}}$ High Time Before Read(See Note)	MIN	70	ns
tRB1	RY/$\overline{\text{BY}}$ Recovery Time(to $\overline{\text{CE}}$, $\overline{\text{OE}}$ go low)	MIN	0	ns
tRB2	RY/$\overline{\text{BY}}$ Recovery Time(to $\overline{\text{WE}}$ go low)	MIN	50	ns

Note:Not 100% tested

Fig E. RESET TIMING WAVEFORM



DRAM: (NT5DS16M16CS)

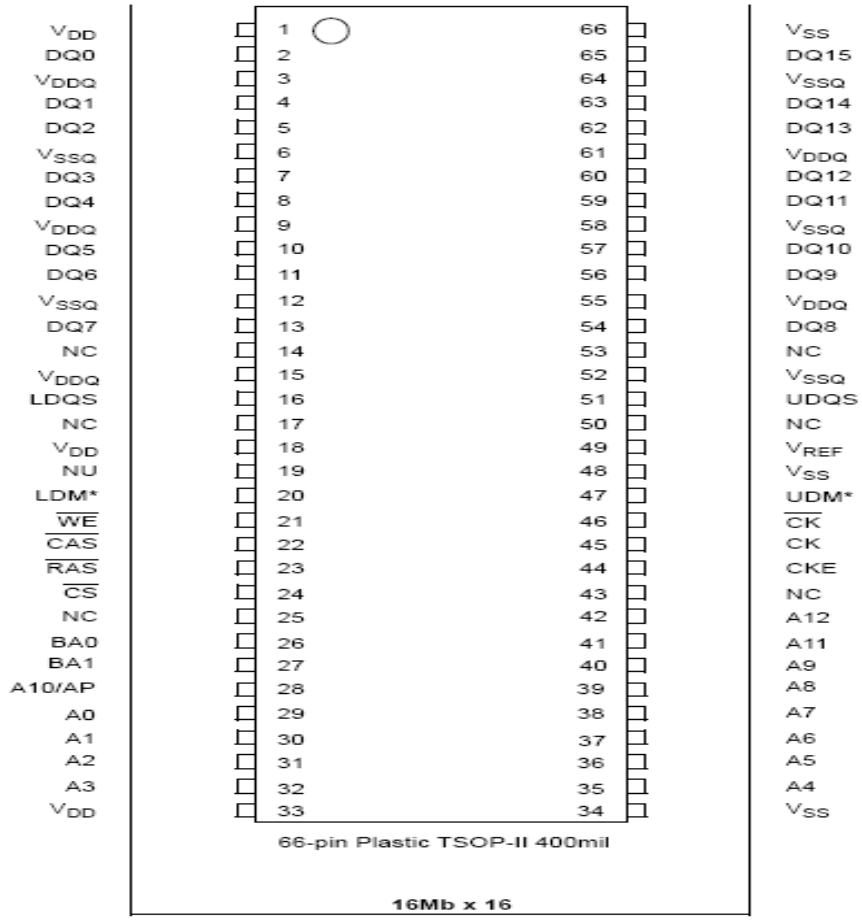
The 256Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268, 435, 456 bits. The 256Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 256Mb DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture
is essentially a *2n* prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 256Mb DDR SDRAM consists of a single *2n*-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

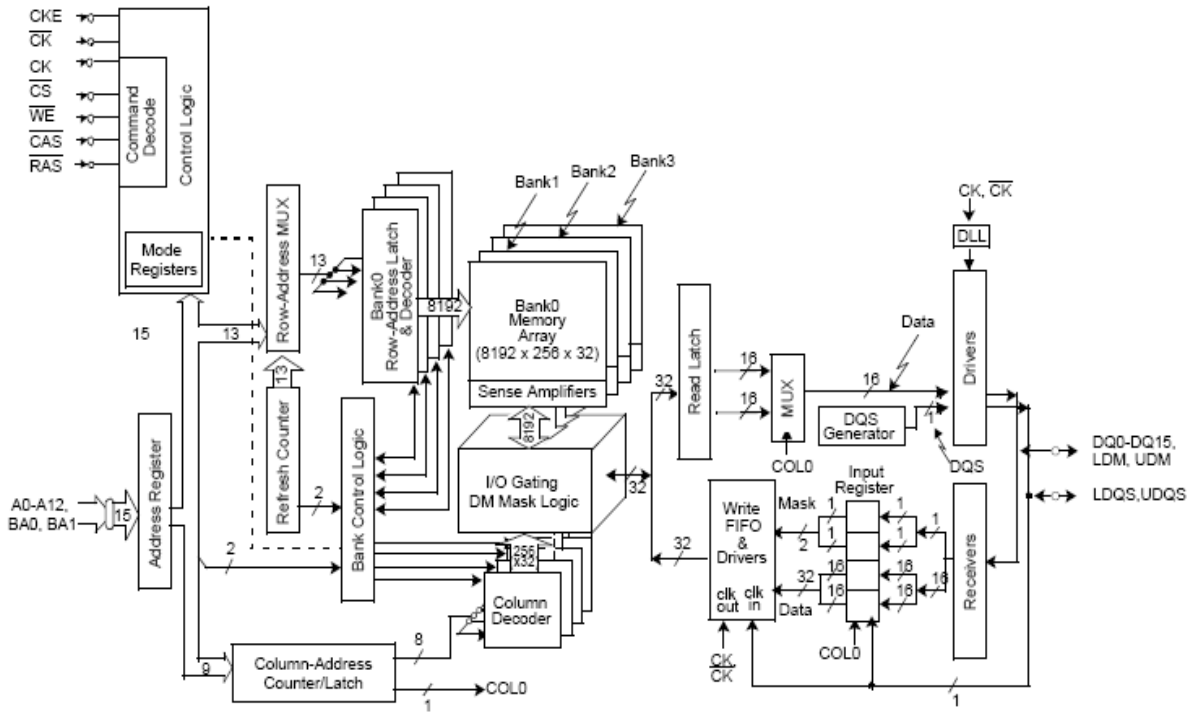
1. Pin Configuration



2. Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE, CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self Refresh operation (all banks idle), or Active Power Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during self refresh. The standard pinout includes one CKE pin. Optional pinouts might include CKE1 on a different pin, in addition to CKE0, to facilitate independent power down control of stacked devices.
$\overline{CS}$, $\overline{CS0}$, $\overline{CS1}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. The standard pinout includes one $\overline{CS}$ pin. Optional pinouts might include $\overline{CS1}$ on a different pin, in addition to $\overline{CS0}$, to allow upper or lower deck selection on stacked devices.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. During a Read, DM can be driven high, low, or floated.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A12	Input	**Address Inputs:** Provide the row address for Active commands, and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 low) or all banks (A10 high). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a Mode Register Set command.
DQ	Input/Output	**Data Input/Output:** Data bus.
DQS, LDQS, UDQS	Input/Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15
NC		**No Connect:** No internal electrical connection is present.
NU		Electrical connection is present. Should not be connected at second level of assembly.
V_{DDQ}	Supply	**DQ Power Supply:** 2.5V ± 0.2V.
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 2.5V ± 0.2V.
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**SSTL_2 reference voltage:** (V_{DDQ} / 2) ± 1%.

3. Block Diagram



Note: This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Note: DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

4. Initialization

Only one of the following two conditions must be met.

• No power sequencing is specified during power up or power down given the following criteria:

VDD and VDDQ are driven from a single power converter output

VTT meets the specification

A minimum resistance of 42 ohms limits the input current from the VTT supply into any pin and VREF tracks VDDQ /2 or The following relationships must be followed:

VDDQ is driven after or with VDD such that VDDQ < VDD + 0.3V

VTT is driven after or with VDDQ such that VTT < VDDQ + 0.3V

VREF is driven after or with VDDQ such that VREF < VDDQ + 0.3V

The DQ and DQS outputs are in the High-Z state, where they remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200µs delay prior to applying an executable command.

Once the 200µs delay has been satisfied, a Deselect or NOP command should be applied, and CKE must be brought HIGH. Following the NOP command, a Precharge ALL command must be applied. Next a Mode Register Set command must be issued for the Extended Mode Register, to enable the DLL, then a Mode Register Set command must be issued for the Mode Register, to reset the DLL, and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. A Precharge ALL command should be applied, placing the device in the “all banks idle” state Once in the idle state, two auto refresh cycles must be performed. Additionally, a Mode Register Set command for the Mode Register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed.

Following these cycles, the DDR SDRAM is ready for normal operation.
DDR SDRAM’s may be reinitialized at any time during normal operation by asserting a valid MRS command to either the base or extended mode registers without affecting the contents of the memory array. The contents of either the mode register or extended mode register can be modified at any valid time during device operation without affecting the state of the internal address refresh counters used for device refresh.

5. Register Definition

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Bus
0*	0*	Operating Mode						CAS Latency			BT	Burst Length			Mode Register

A12 - A9	A8	A7	A6 - A0	Operating Mode
0	0	0	Valid	Normal operation Do not reset DLL
0	1	0	Valid	Normal operation in DLL Reset
0	0	1	VS**	Vendor-Specific Test Mode
–	–	–		Reserved

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (Option)
1	0	0	Reserved
1	0	1	1.5 (Option)
1	1	0	2.5
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

VS** Vendor Specific

* BA0 and BA1 must be 0, 0 to select the Mode Register (vs. the Extended Mode Register).

6. Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-A i selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-A i selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-A i selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in *Burst Definition* on page 11.

Read Latency

The Read latency, or CAS latency, is the delay, in clock cycles, between the registration of a Read command and the availability of the first burst of output data. The latency can be

programmed 2 or 2.5 clocks.
If a Read command is registered at clock edge n, and the latency is *m* clocks, the data is available nominally coincident with clock edge *n* + m. Reserved states should not be used as unknown operation or incompatibility with future versions may result..

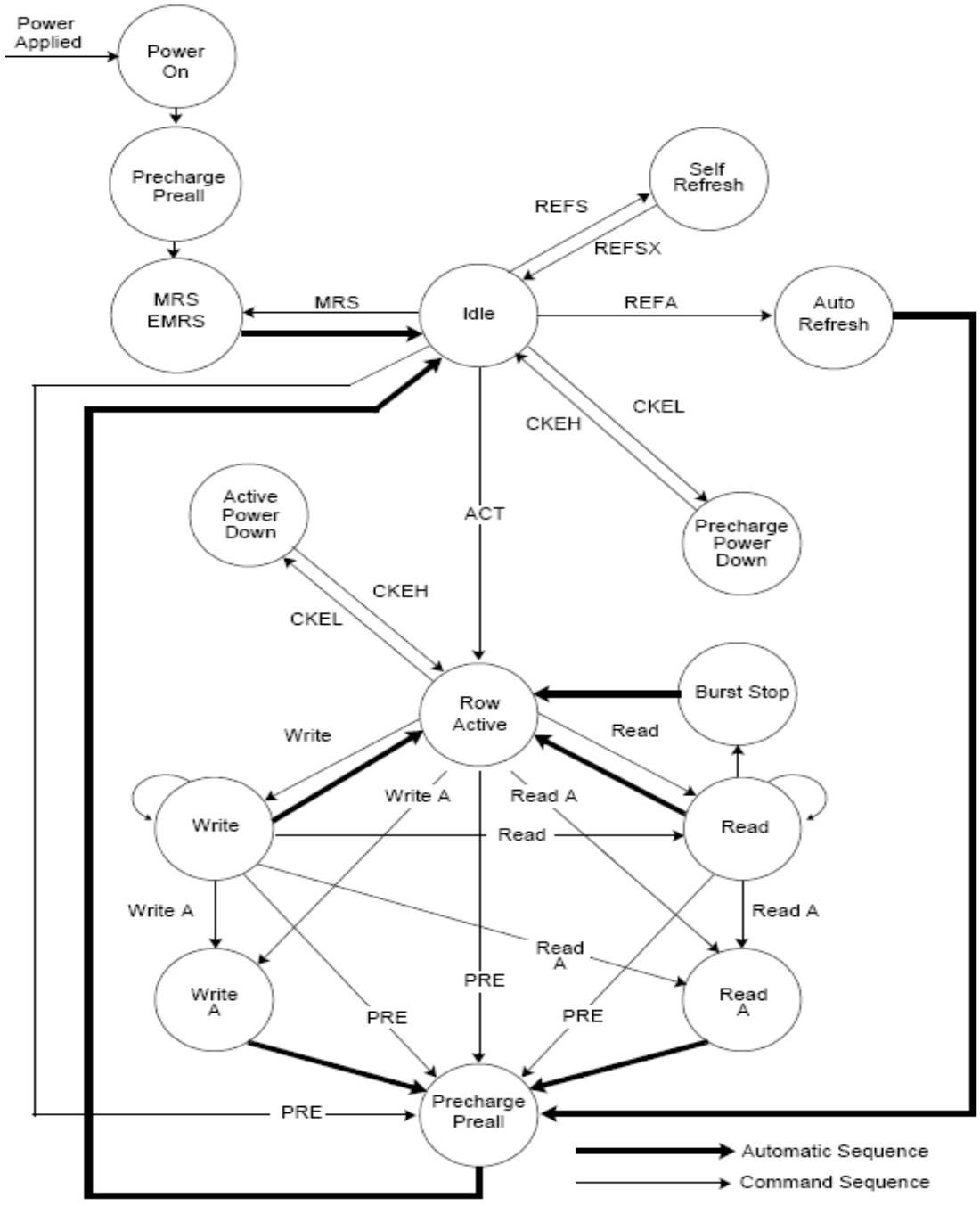
Operating Mode

The normal operating mode is selected by issuing a Mode Register Set Command with bits A7-A12 to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a Mode Register Set command with bits A7 and A9-A12 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. A Mode Register Set command issued to reset the DLL should always be followed by a Mode Register Set command to select normal operating mode. All other combinations of values for A7-A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used as unknown operation or incompatibility with future versions may result.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before a Read command can be issued. This is the reason for introducing timing parameter tXSRD for DDR SDRAM's (Exit Self Refresh to Read Command). Non- Read commands can be issued 2 clocks after the DLL is enabled via the EMRS command (tMRD) or 10 clocks after the DLL is enabled via self refresh exit command (tXSNR, Exit Self Refresh to Non-Read Command).

7. Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

8. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	−0.5 to V_{DDQ}+ 0.5	V
V_{IN}	Voltage on Inputs relative to V_{SS}	−0.5 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	−0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	−0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to +150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

9. Capacitance

Parameter	Symbol	Min.	Max.	Units	Notes
Input Capacitance: CK, $\overline{CK}$	CI_1	2.0	3.0	pF	1
Delta Input Capacitance: CK, $\overline{CK}$	delta CI_1		0.25	pF	1
Input Capacitance: All other input-only pins (except DM)	CI_2	2.0	3.0	pF	1
Delta Input Capacitance: All other input-only pins (except DM)	delta CI_2		0.5	pF	1
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF	1, 2
Delta Input/Output Capacitance: DQ, DQS, DM	delta C_{IO}		0.5	pF	1

1. $V_{DDQ} = V_{DD} = 2.5V \pm 0.2V$ (minimum range to maximum range), f = 100MHz, $T_A = 25°C$, $VO_{DC} = V_{DDQ/2}$, $VO_{Peak\text{-}Peak} = 0.2V$.
2. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match input propagation times of DQ, DQS and DM in the system.

10. DC Electrical Characteristics and Operating Conditions

(0°C £ TA £ 70×C; V_{DDQ} = 2.5V ± 0.2V, V_{DD} = + 2.5V ± 0.2V, see AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage	2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)	V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
$V_{IH(DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL(DC)}$	Input Low (Logic0) Voltage	– 0.3	V_{REF} – 0.15	V	1
$V_{IN(DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs	– 0.3	V_{DDQ} + 0.3	V	1
$V_{ID(DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
$V_{IX(DC)}$	Input Crossing Point Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
VI_{Ratio}	V-I Matching Pullup Current to Pulldown Current Ratio	0.71	1.4		5
I_I	Input Leakage Current Any input 0V ≤ V_{IN} ≤ V_{DD}; (All other pins not under test = 0V)	– 5	5	µA	1
I_{OZ}	Output Leakage Current (DQs are disabled; 0V ≤ V_{out} ≤ V_{DDQ}	– 5	5	µA	1
I_{OH}	Output Current: Nominal Strength Driver High current (V_{OUT}= V_{DDQ} -0.373V, min V_{REF}, min V_{TT}) Low current (V_{OUT}= 0.373V, max V_{REF}, max V_{TT})	– 16.8		mA	1
I_{OL}		16.8			

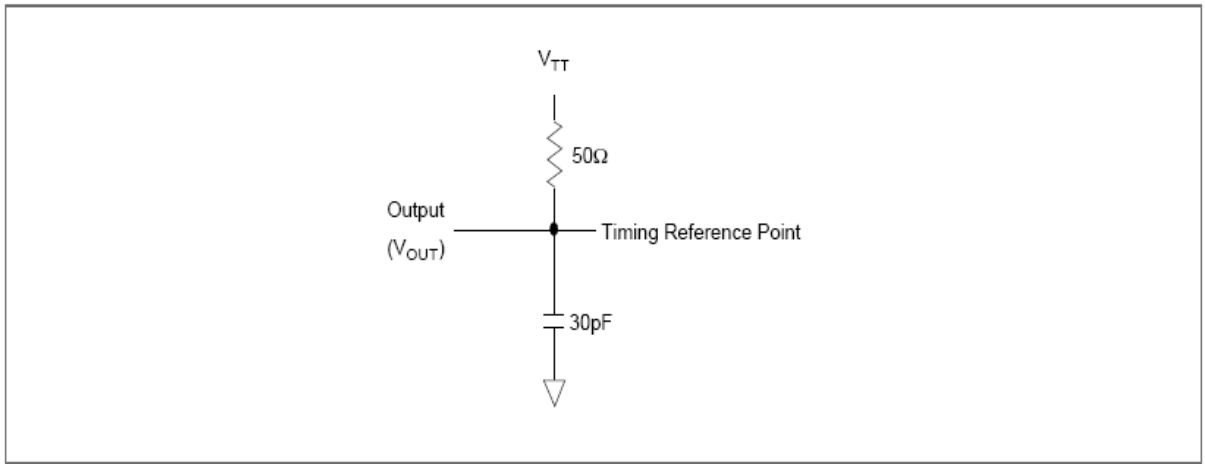
Symbol	Parameter	Min	Max	Units	Notes
I_{OHW}	Output Current: Half- Strength Driver High current (V_{OUT}= V_{DDQ} -0.763V, min V_{REF}, min V_{TT}) Low current (V_{OUT}= 0.763V, max V_{REF}, max V_{TT})	– 9.0		mA	1
I_{OLW}		9.0			

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages for 0.25 volts to 1.0 volts. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

11. AC Characteristics

1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK, CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input low (high) level.

AC Output Load Circuit Diagrams



AC Input Operating Conditions

(0 °C ≤ TA ≤ 70 °C; VDDQ = VDD = 2.5V ± 0.2V (DDR333); VDDQ = VDD = 2.6V ± 0.1V (DDR400); See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage, DQ, DQS, and DM Signals	V_{REF} + 0.31		V	1, 2
$V_{IL(AC)}$	Input Low (Logic 0) Voltage, DQ, DQS, and DM Signals		V_{REF} – 0.31	V	1, 2
$V_{ID(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX(AC)}$	Input Crossing Point Voltage, CK and $\overline{CK}$ Inputs	0.5*V_{DDQ} – 0.2	0.5*V_{DDQ} + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

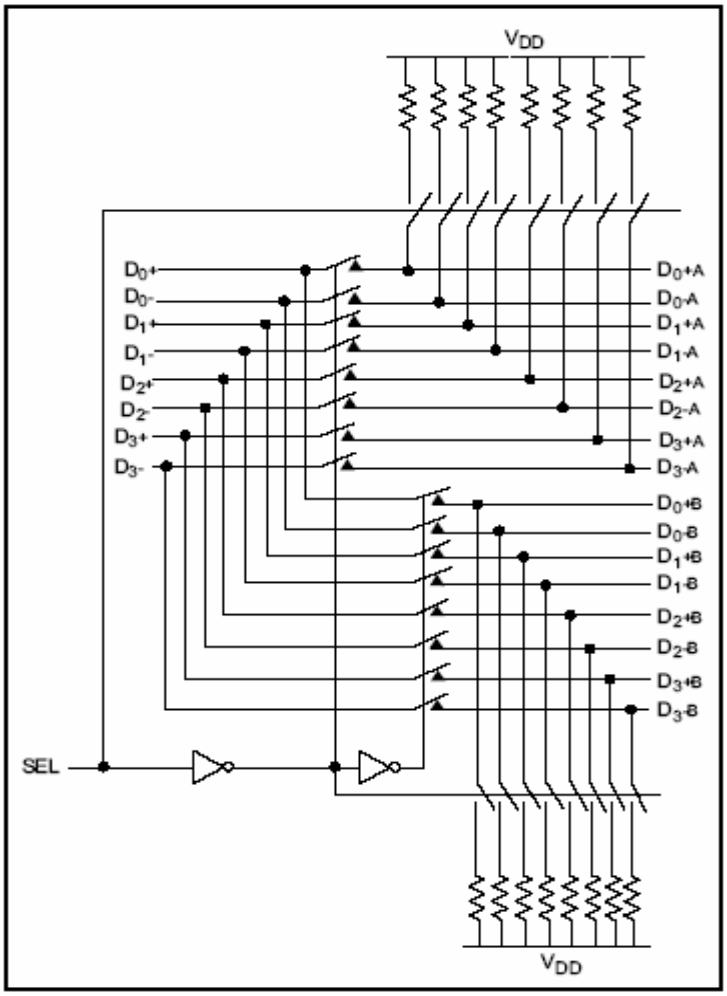
PI3HDMI412FT-A

Pericom Semiconductor's PI3HDMI series of switch circuits are targeted for high-resolution video networks that are based on DVI/HDMI standards, and TMDS signal processing. The PI3HDMI412FT-A is an 8- to 4-Channel Mux/DeMux Switch. The device multiplexes differential signals to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation.

The allowable data rate of 5.0Gbps provides the resolution required by the next generation HDTV and PC graphics. Three differential channels are used for data (video signals for DVI or audio/video signals for HDMI), and one differential channel is used for Clock for decoding the TMDS signals at the outputs.

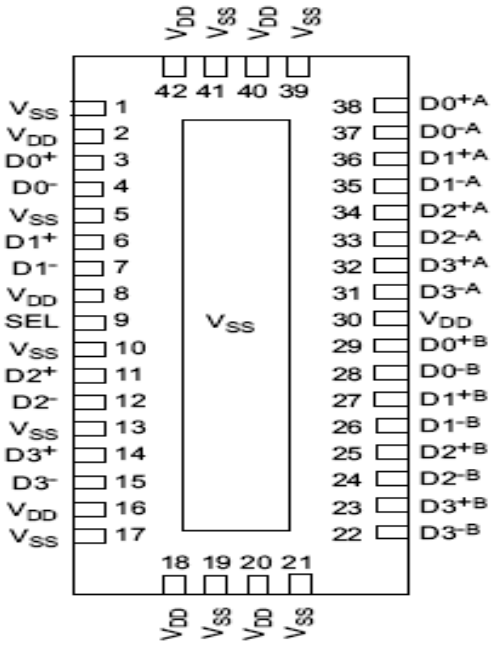
Because of its passive bidirectional feature, this switch can be used either at the video drivers side or at the receiver side. For PC graphics applications, the device sits at the drivers side to switch between multiple display units such as PC LCD monitor, projector, TV, etc. For consumer video applications, the device sits at the receiver end to switch between the source components such as DVD, D-VHS, STB, etc.

Block Diagram



Pin Description

42-pin TQFN



Pin Description

Pin # (BQSOP)	Pin # (TQFN)	Pin Name	Description
2, 4, 12, 21, 23, 25, 36, 48	2, 8, 16, 18, 20, 30, 40, 42	V_{DD}	+ Power supply 3.30
1, 3, 5, 8, 11, 14, 17, 20, 22, 24, 26, 31, 37, 42, 47	1, 5, 10, 13, 17, 19, 21, 39, 41	V_{SS}	- Power supply
13	9	SEL	Select pin, see truth table
6, 7, 9, 10, 15, 16, 18, 19, 27-30, 32-35, 38-41, 43-46	3, 4, 6, 7, 11, 12, 14, 15, 22-29, 31-38,	$Dx^{+/-x}$ + $CLK^{+/-x}$	Data + Clk bits for TMDS signal

Maximum Ratings

Storage Temperature	–65°C to +150°C
Supply Voltage to V_{SS} Potential	–0.5V to +2.5V
DC Input Voltage	V_{SS} to V_{DD}
DC Output Current	120mA

DC Power Supply Characteristics

Paramenter	Description	Min.	Max.	Units
V_{DD}	Positive Power Supply	3.0	3.6	V
V_{SS}	Negative Power Supply	1.5	1.6	V

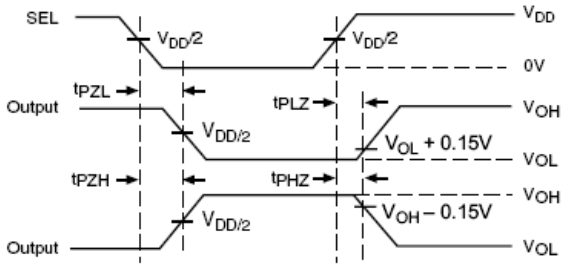
Power Supply Characteristics

Parameters	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{DD} = Max., V_{IN} = V_{DD} or V_{SS}		200		µA

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at TA = 25°C ambient and maximum loading.

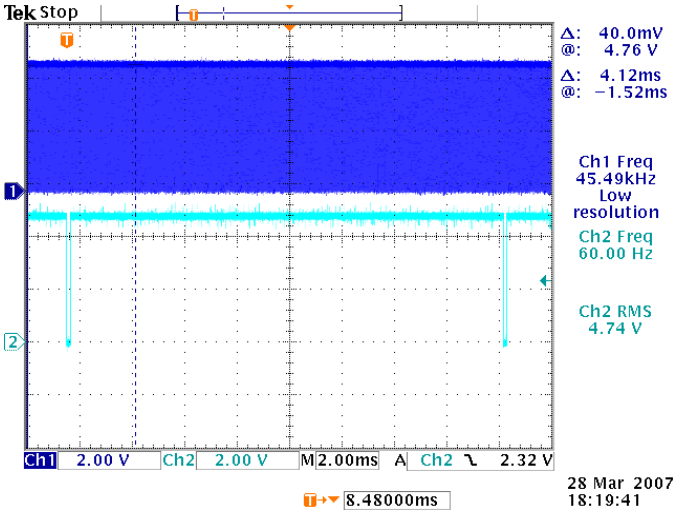
Switching Waveforms



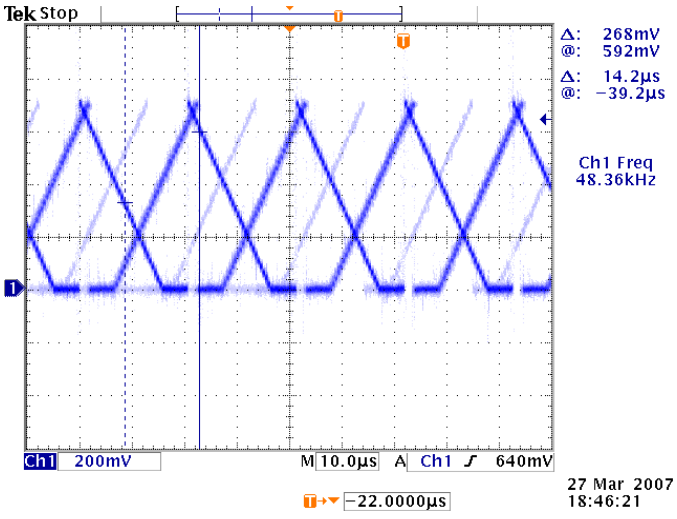
Chapter8 Waveforms

PC MODE(1024X768 60HZ)

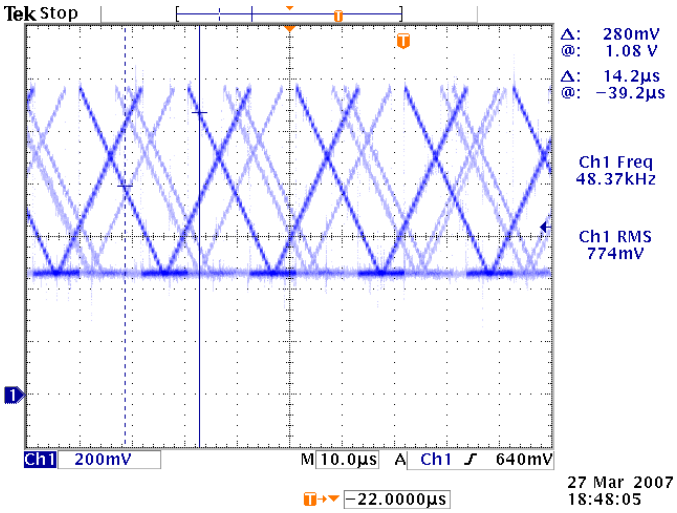
CH1 H-sync (R209); CH2 V-sync (R213)



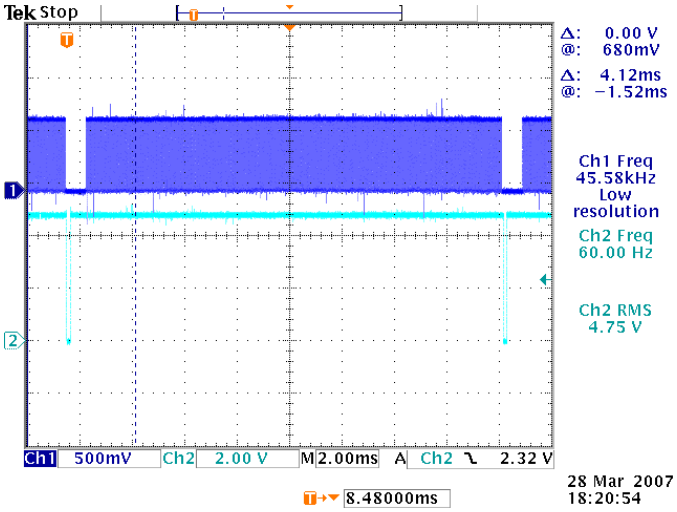
CH1 GRN (R195) (pattern: 32 gary)



CH1 GP (C89) (pattern: 32 gary)

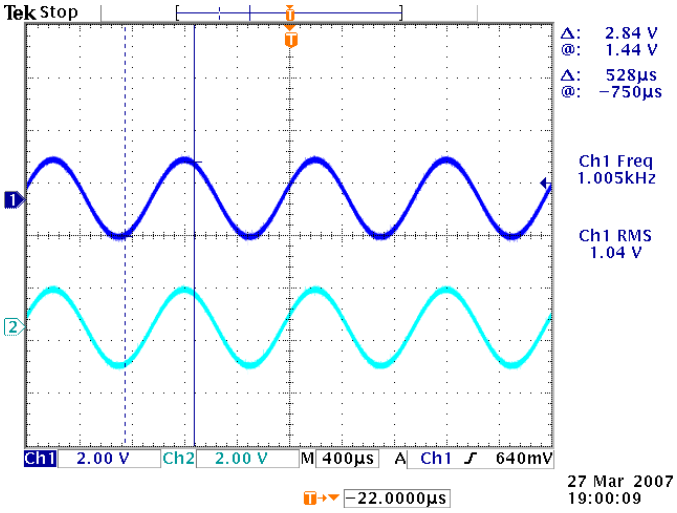


CH1 GREEN # (R195); CH2 VGA VSYNC (R213)



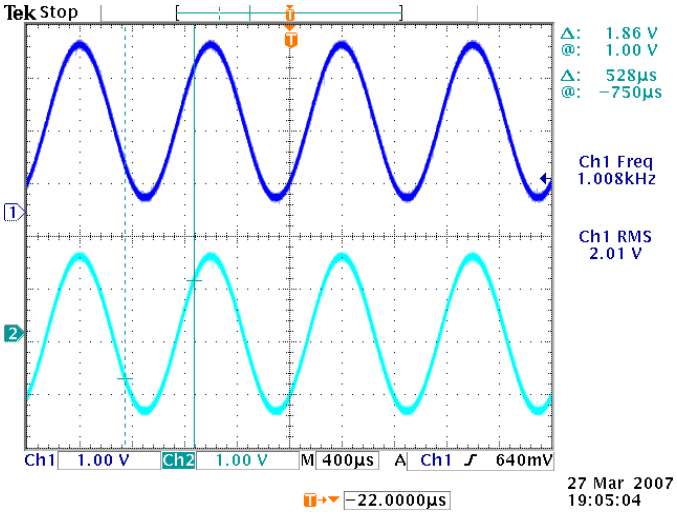
CH1 VGAL_IN (R208); CH2 VGAR_IN (R207) [Audio]

input: 1KHZ ;1Vrms



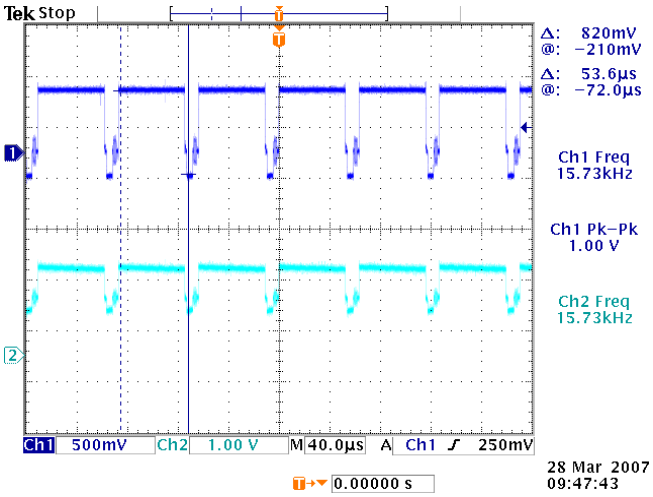
CH1 VGAL_IN (CE56+) ; VGAL_IN (CE56-)

input: 1KHZ ;1Vrms



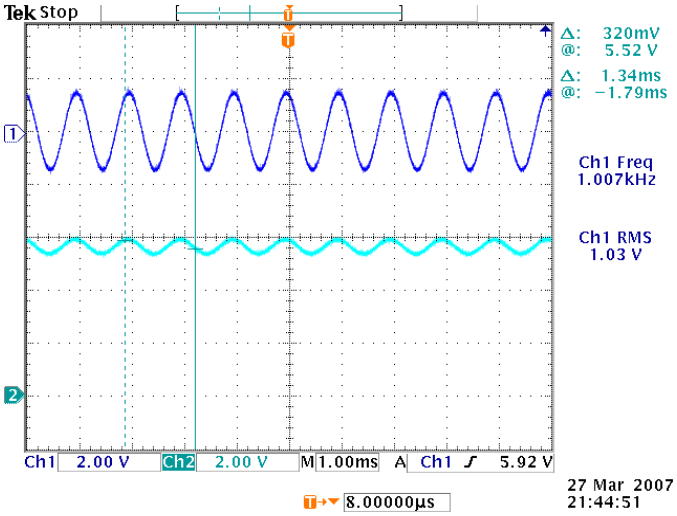
AV&ATV MODE (AV1/AV2/TV) VIDEO (pattern: full white)

CH1 CVBS2 (R146); CH2 AV2CVBS (C52)

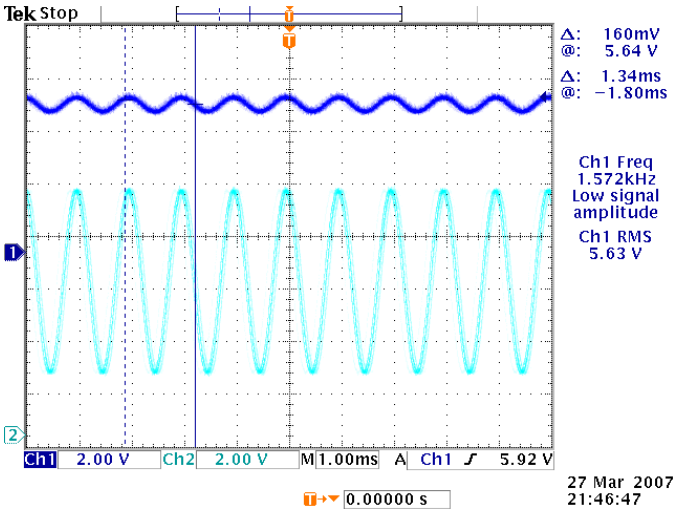


CH1 AV1L (CE64-); CH2 VOUT1L (U28 PIN25) [Audio]

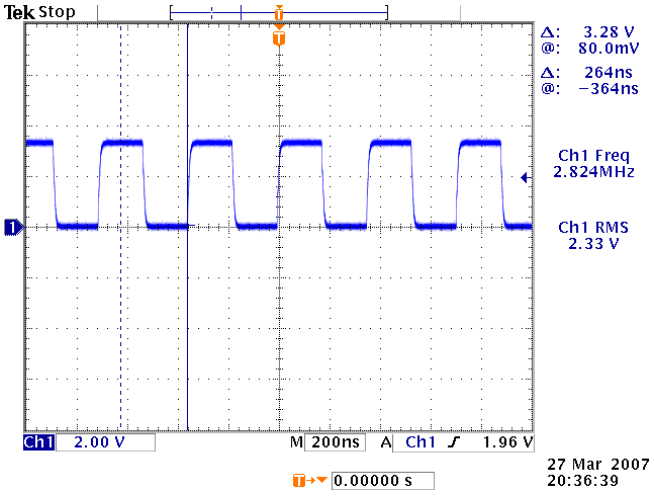
input: 1KHZ ;1Vrms



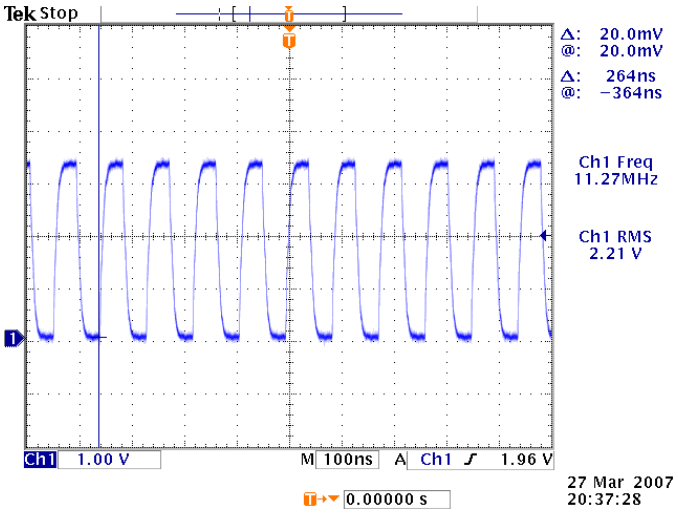
CH1 A01AUXL (R335);CH2 OUT2+ 17(J6 PIN4)



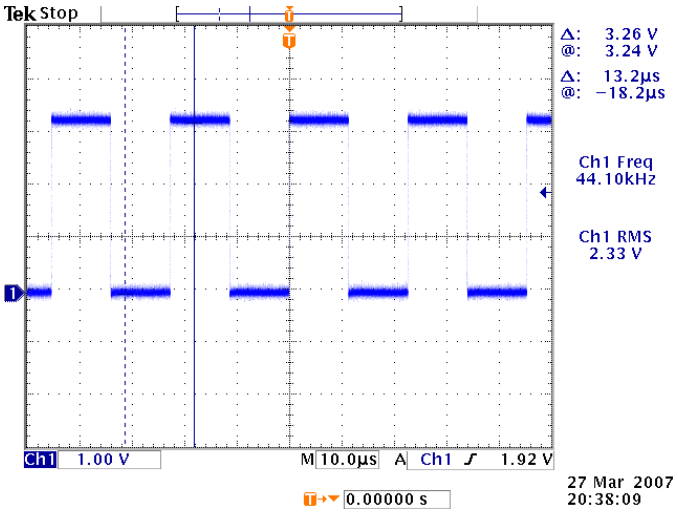
CH1 DAC BCLK0 (U28 PIN4);



CH1 DAC MCLK0 (U28 PIN6);

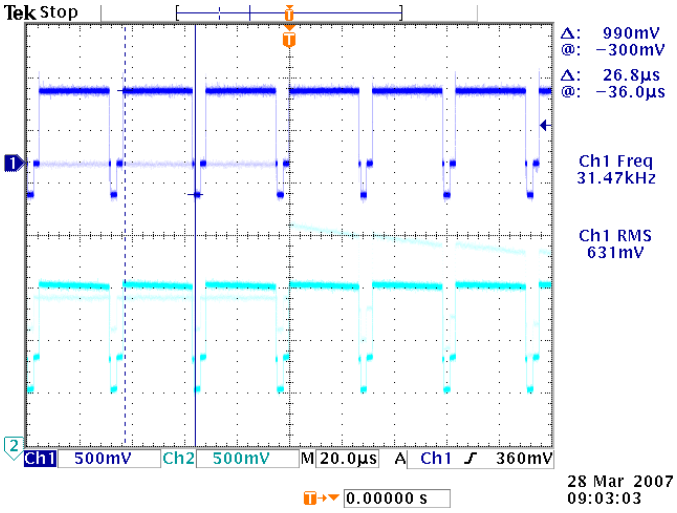


CH1 DAC LRCK0 (U28 PIN5)



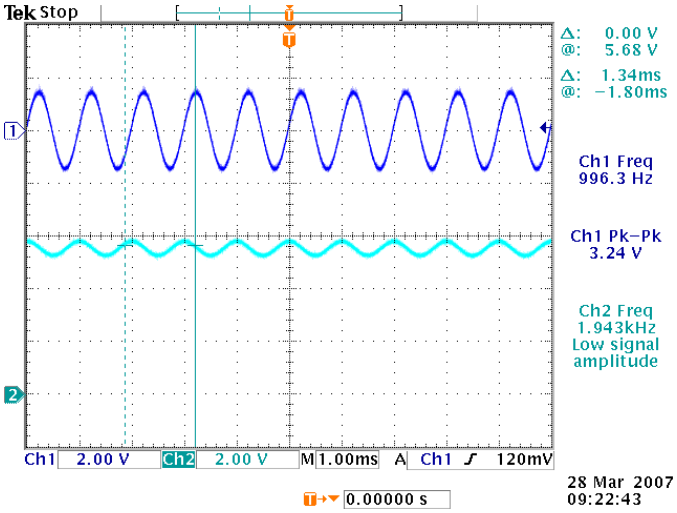
COMPONENT MODE (COMPONENT 1/2) (480P) (pattern: full white)

CH1 Y1_IN (R180); CH2 Y1P (C77)



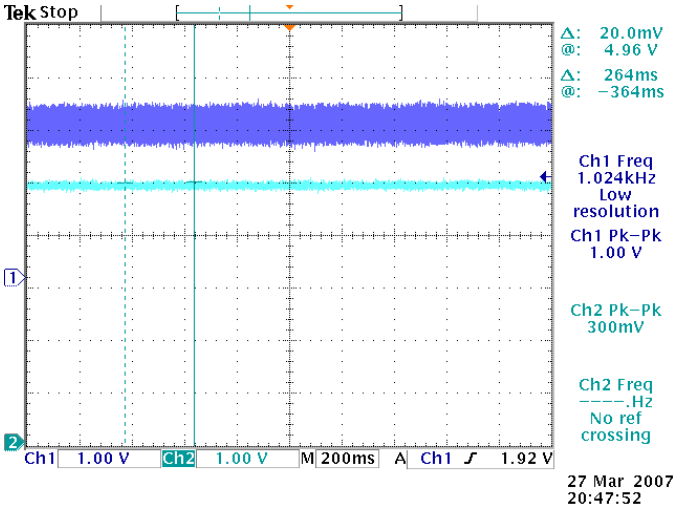
CH1 YPBPR0L_IN (CE47(-)) CH2 VOUT1L (U28 PIN25)

input: 1KHZ ;1Vrms

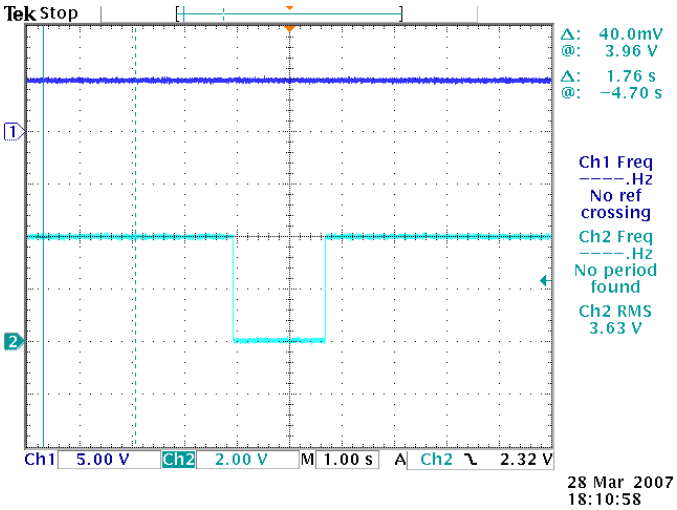


HDMI 1&2 (1080i) (pattern: white)

CH1 RX0_2 (P6 PIN 1); CH2 PWR5V_0 (P6 PIN18)

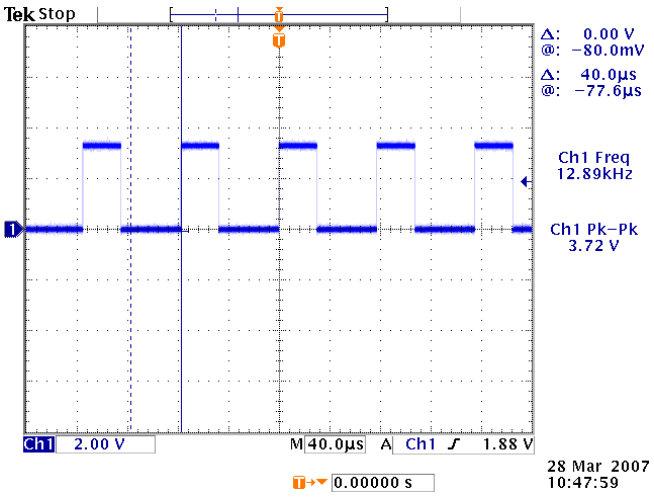


CH1 HDMIDDCSCL_0(R235) ; CH2 HDMICAB0 (Q8 PIN3)

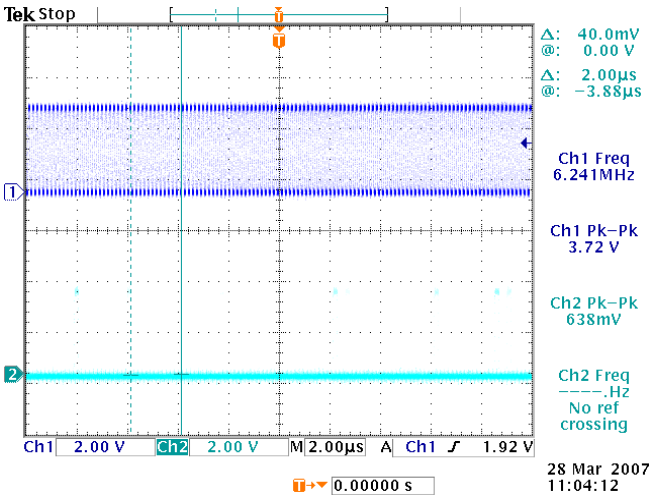


DTV HD

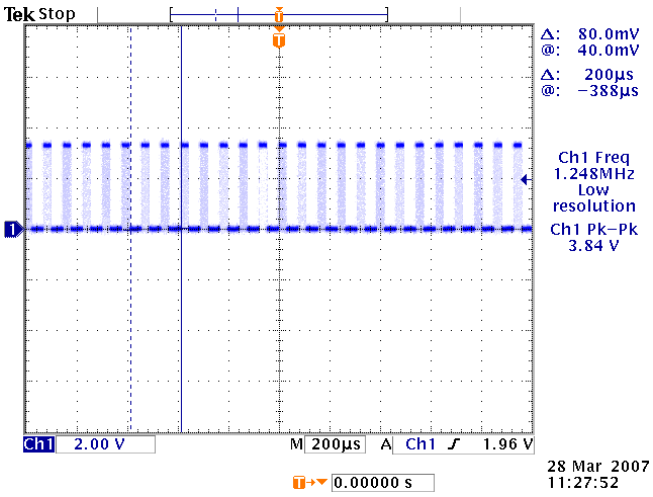
CH1 TS0VALID (RP3 PIN7)



CH1 TS0CLK (RP3 PIN6) CH2 TS0SYNC (RP3 PIN5)

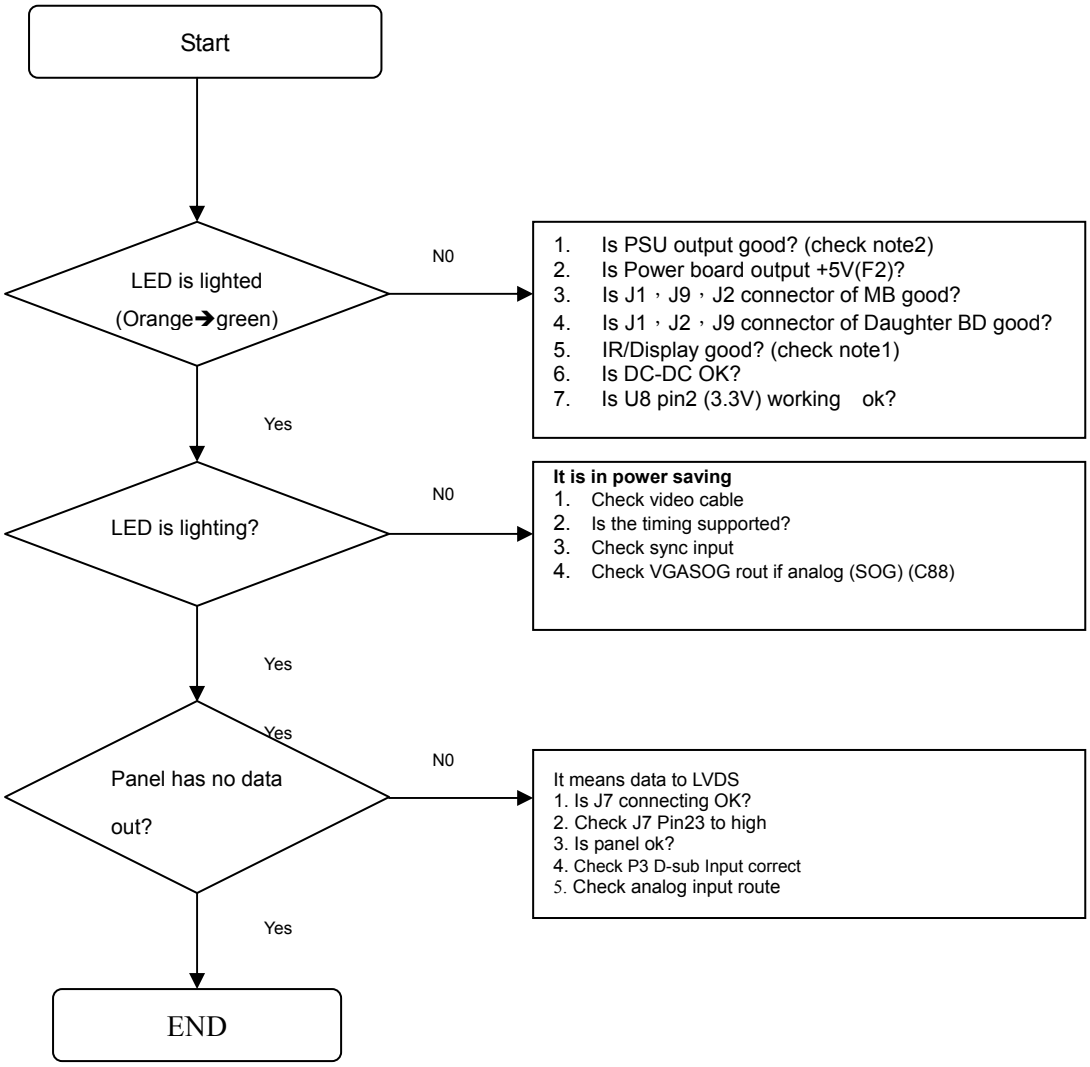


CH1 TS0DATA0 (RP4 PIN8)



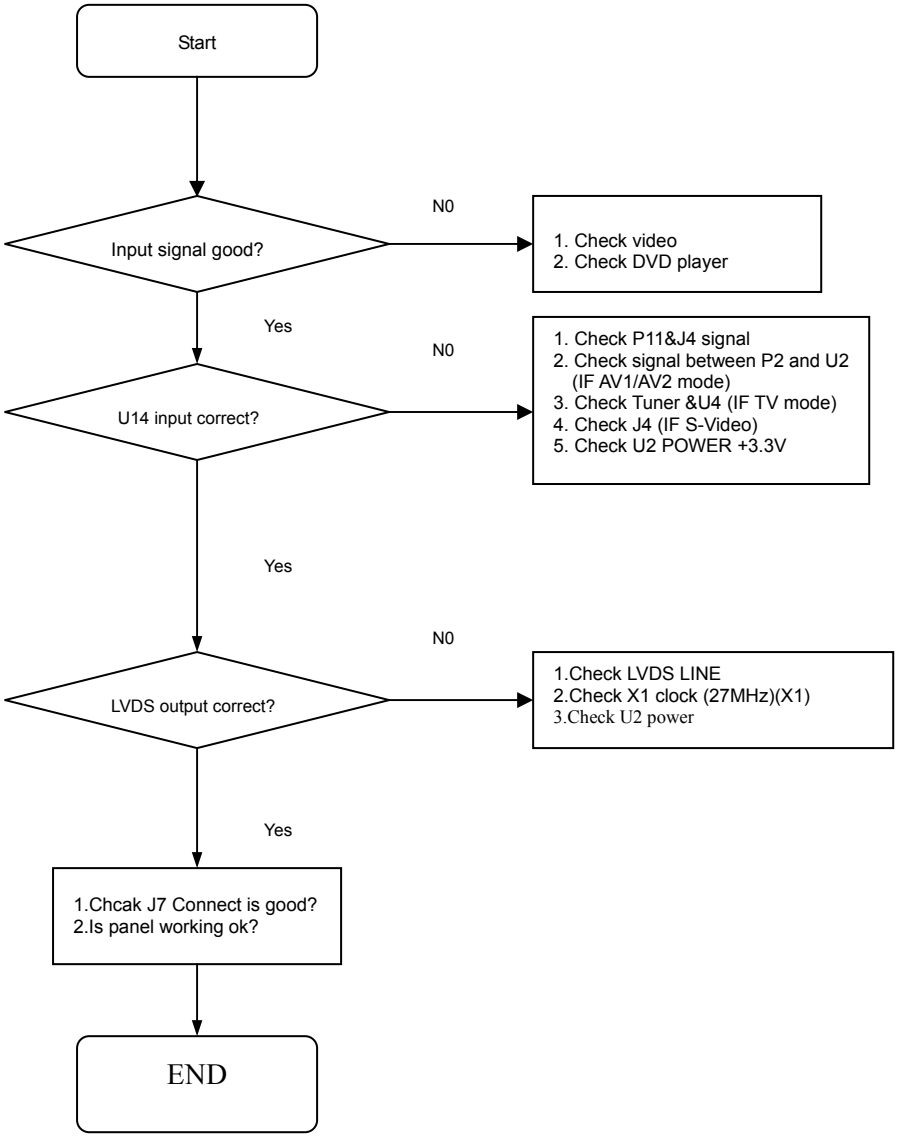
Chapter 9 Trouble solvents

MONITOR DISPLAY NOTHING (PC MODE)

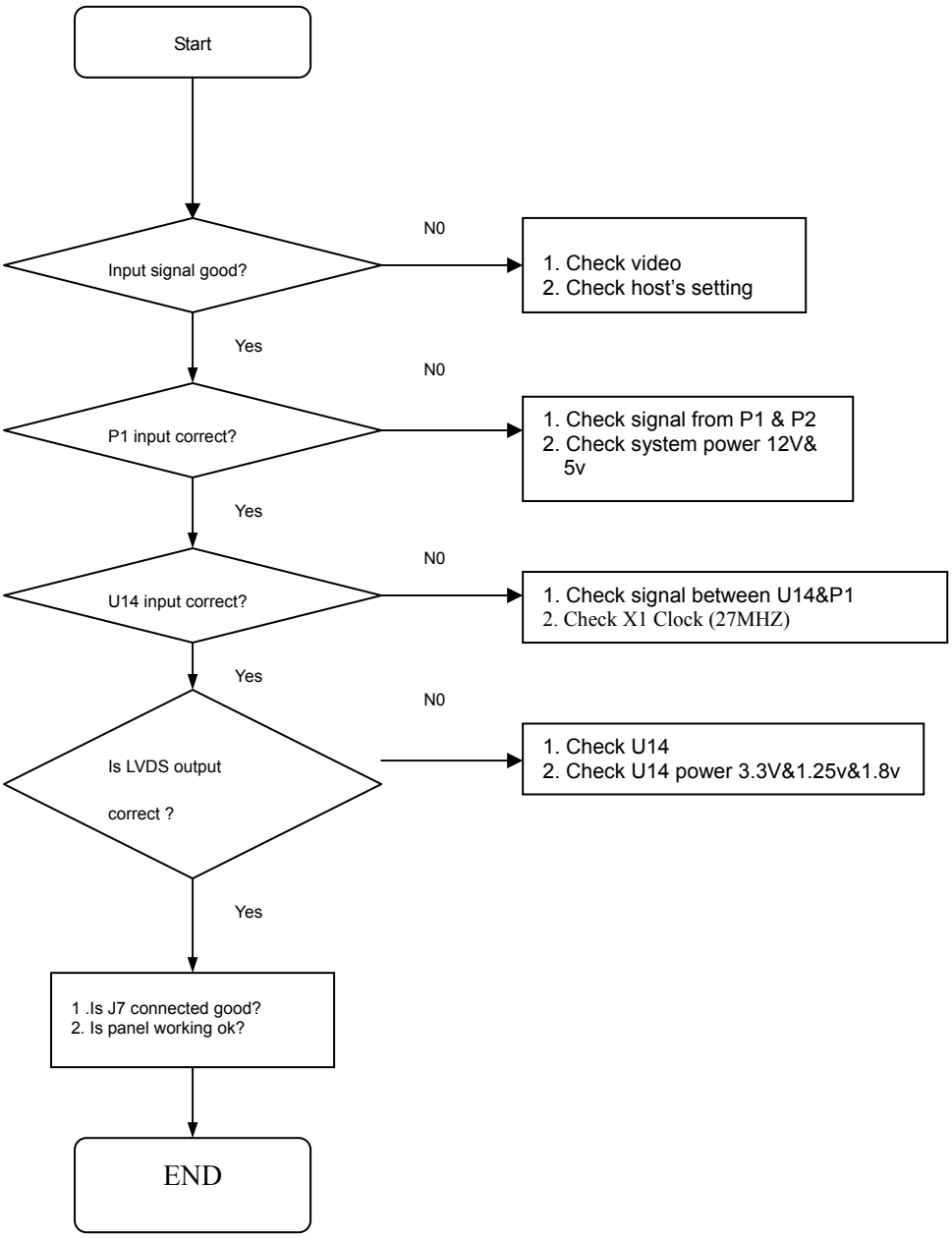


I

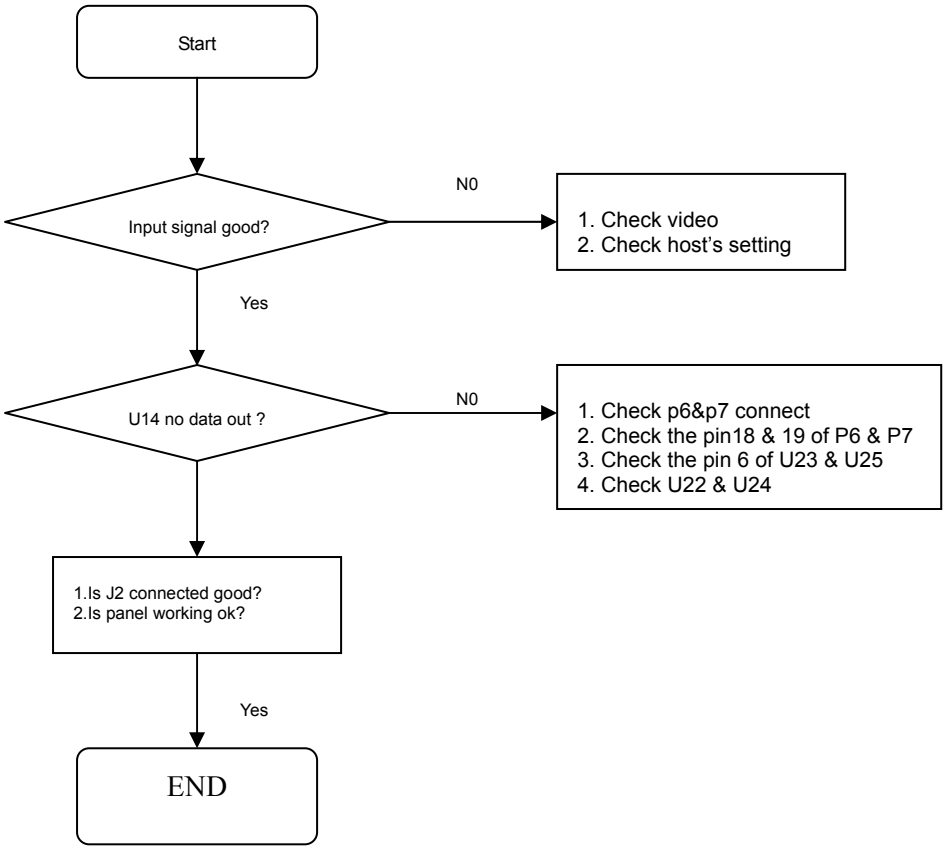
(TV, COMPOSITE VIDEO1, 2, S-VIDEO) IS NOT DISPLAY CORRECTLY



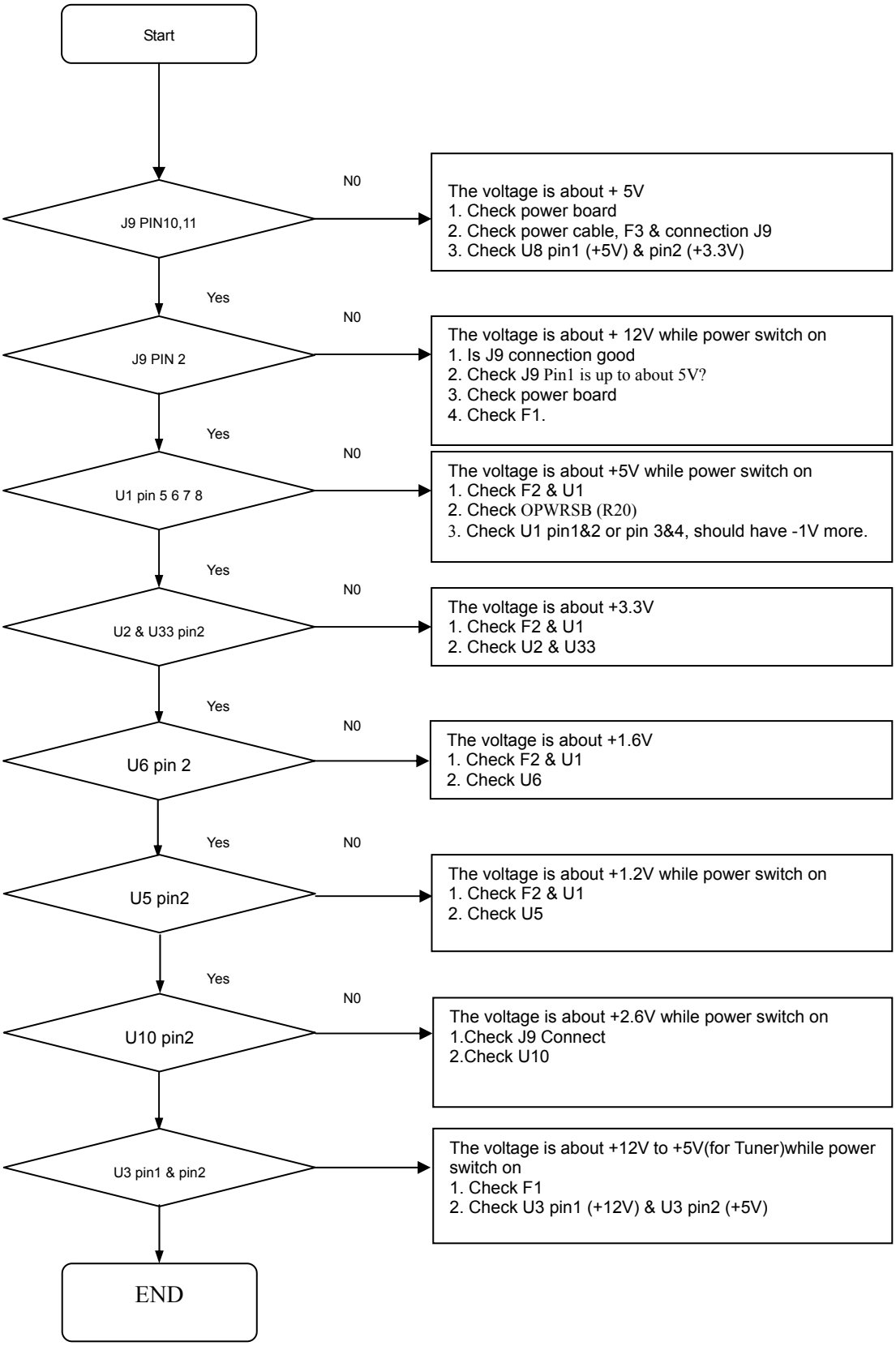
(COMPONENT1, 2) IS NOT DISPLAY CORRECTLY



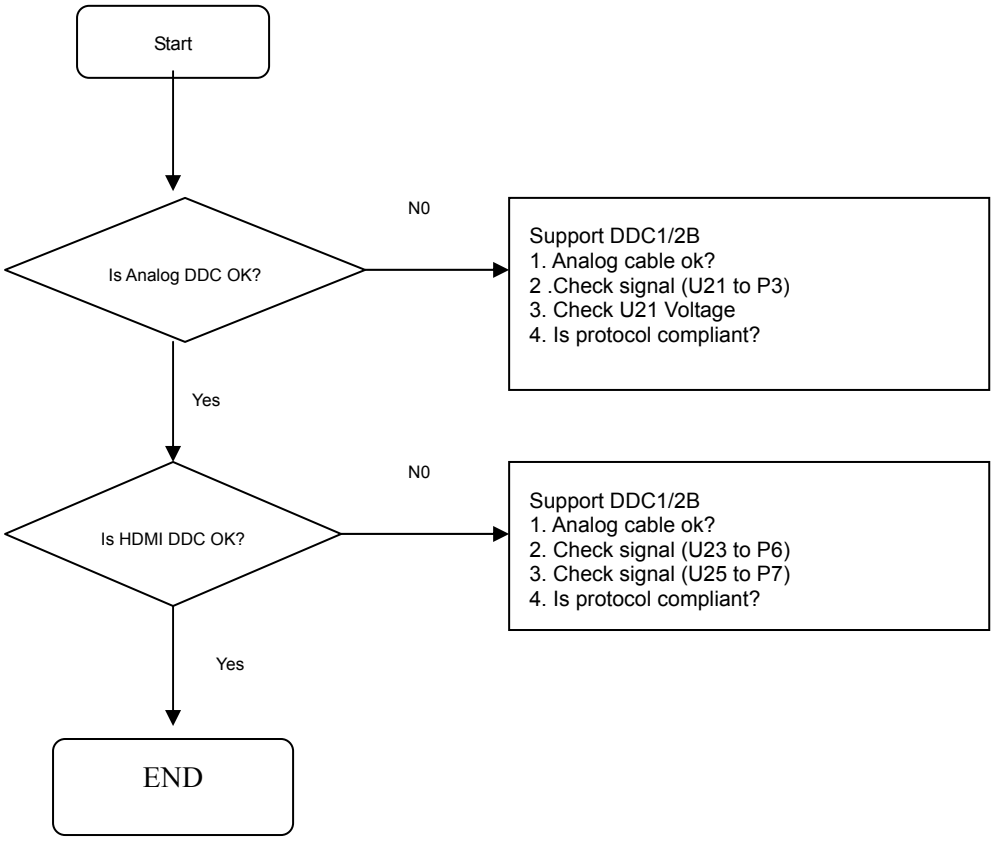
(HDMI) IS NOT DISPLAY CORRECTLY



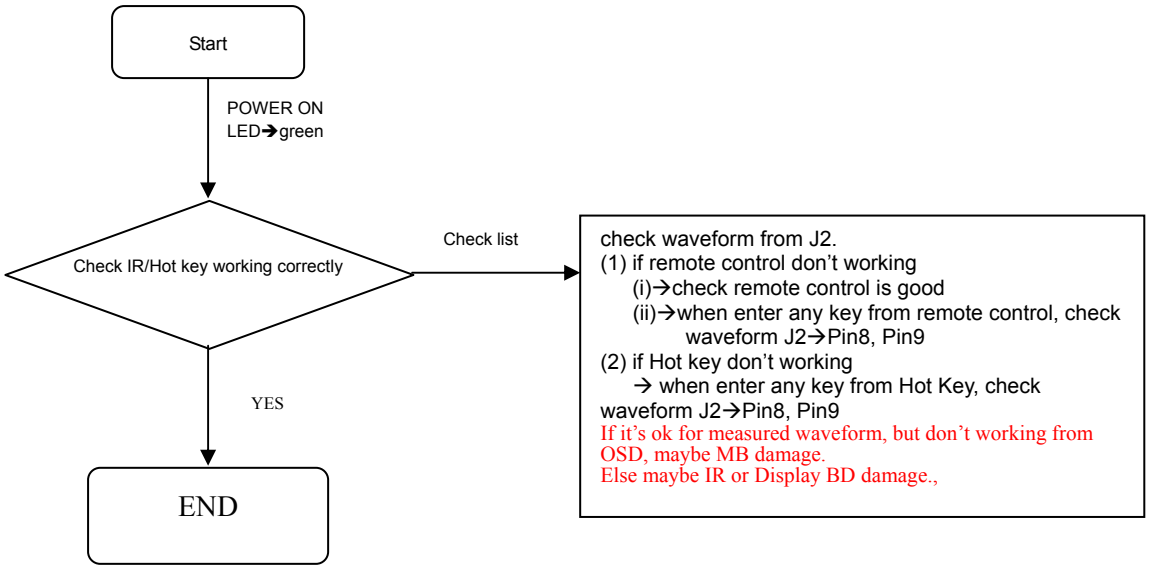
TROUBLE OF DC-DC CONVERTER



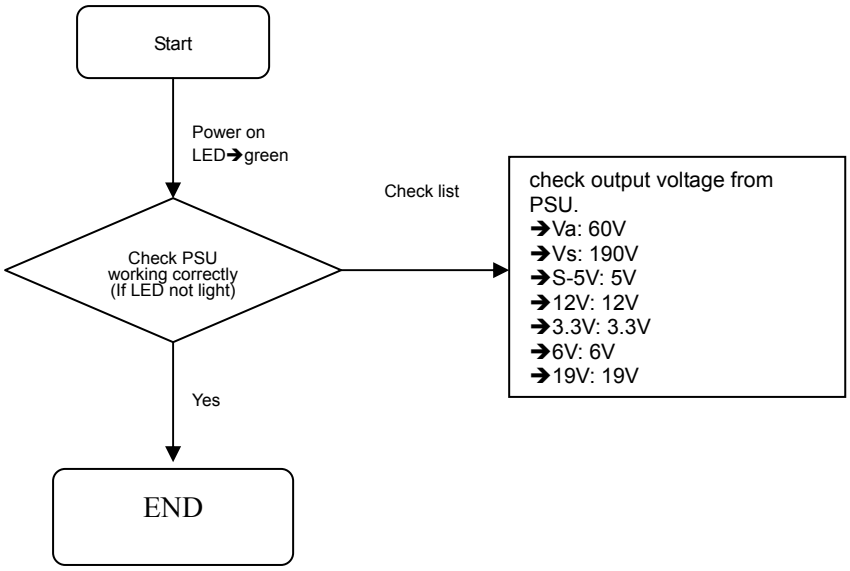
TROUBLE OF EDID READING



NOTE 1: IR/DISPLAY BD NOT WORKING CORRECTLY

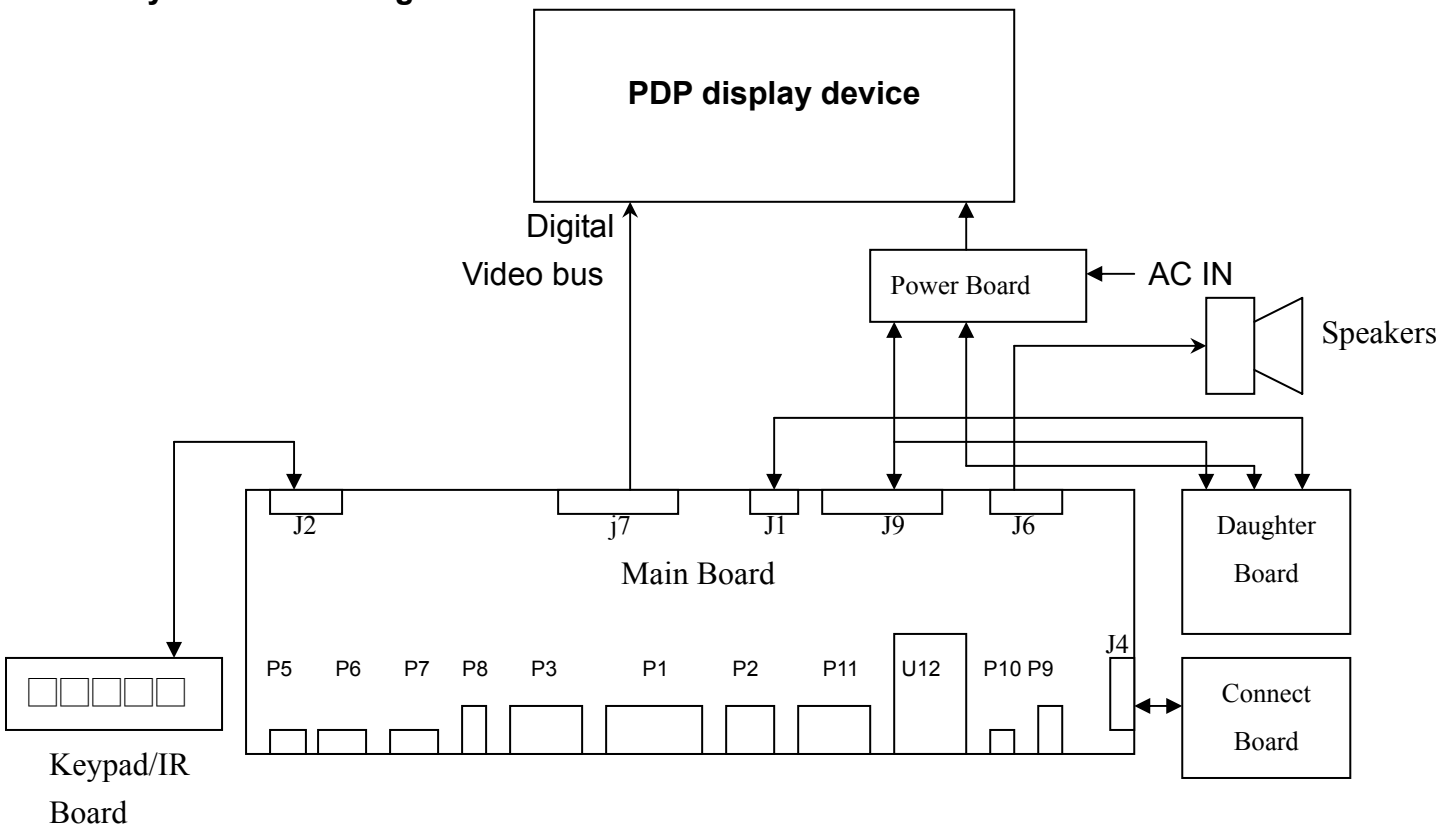


NOTE 2: PSU OF PANEL NOT WORKING CORRECTLY



Chapter 10 Block Diagram

System Block Diagram



Our LCD TV system works at the AC power supplying 100V~240V AC +/- 10% @ 50/60 HZ. The Main Board is supported power by the Power Board, which converts the AC source to the DC 5V & 12V& 24Vsource. The 5V is the system stand-by energy, and the 12V works when we start our system. Indicating LED back light shows the state of our system by its light colors. “Orange” means stand-by, or “White” means working. The 24V supports energy for the inverter, which keeps the LCD back light module stable.

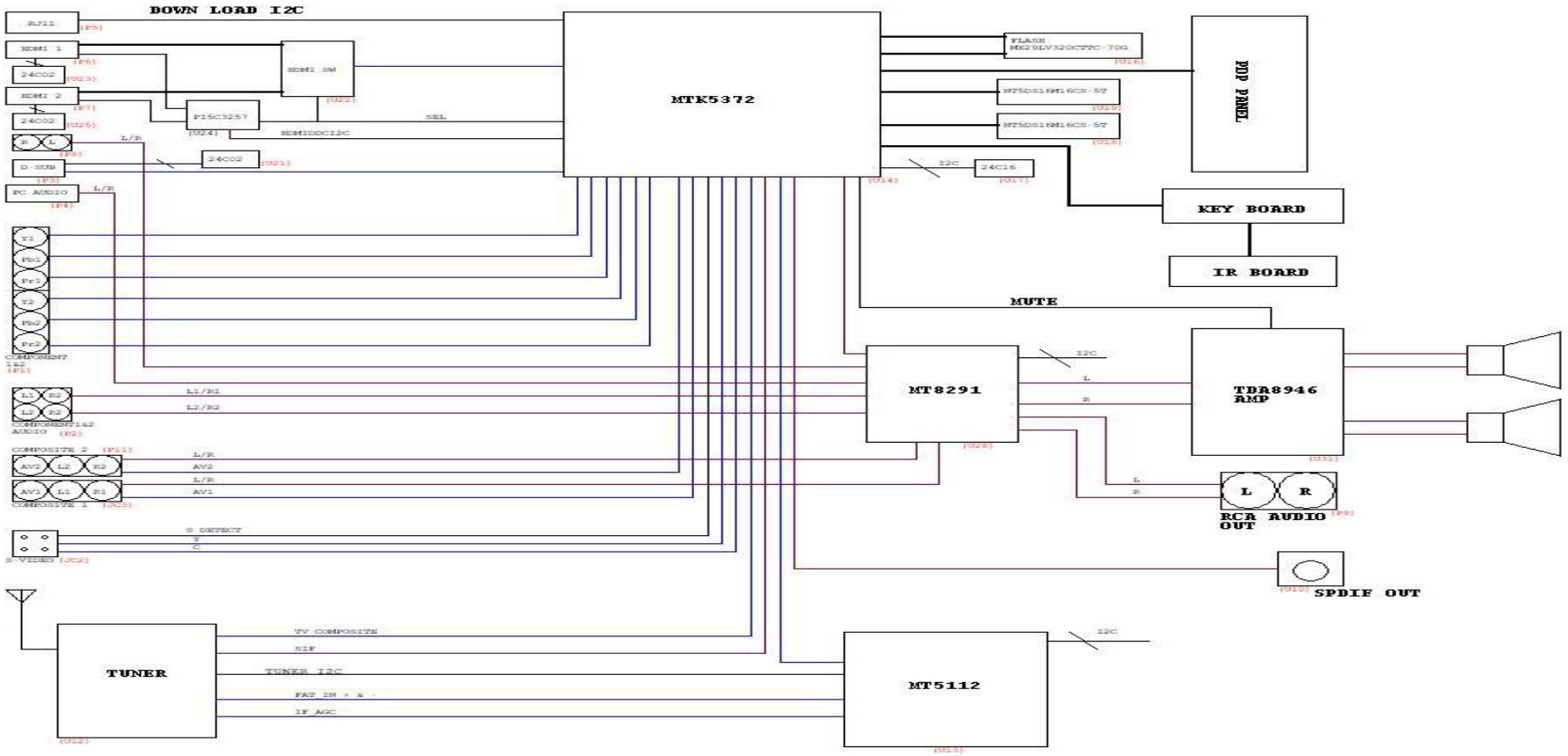
Our LCD TV system, VP42L HDTV20A, supports different kinds of multi-media formats. They are 1x RF (ATSC/QAM/NTSC), Composite Video / S-Video, Analog RGB, Component YPbPr, HDMI1.1 with HDCP and stereo audio outputs. As shown in the figure “main board block diagram”, MT5372 processes video signals and audio signals and MT8291 processes audio signals. MT5372 is also a LVDS generator. The processed video signals are transmitted to panel terminal as LVDS format.

The analog video signals (composite / S-Video, Analog RGB, and YPbPr) are transmitted to MT5372 directly. Their stereo audio signals are transmitted to MT8291.

The RF signals include analog and digital TV signals. Two kinds of signals are processed by two kinds of ways. We introduce the processing way of analog signals, then digitals is similar they. First of all, analog signals are processed by MT5372. The processed signals are divided into two parts, video and audio. Video signals are converted as LVDS and transmitted to the panel terminal. MT8291 processes the processing audio signals, and transmits these signals to audio amplifier. Digital signals are processed by MT5112, a demodulator, firstly. After demodulating, they are processed as the same way as analog signals.

The two ports of HDMI signals pass a HDMI signal switch (PI3HDMI412FT-A). MT5372 processes HDMI signals directly, then transform video signal to LVDS and audio signal to I2S. LVDS are transmitted to LCD device, and I2S signals to U28 (MT8291). The passing signals are processed as other audio signals.
Main broad block diagram shows the routes of these signals in our system.

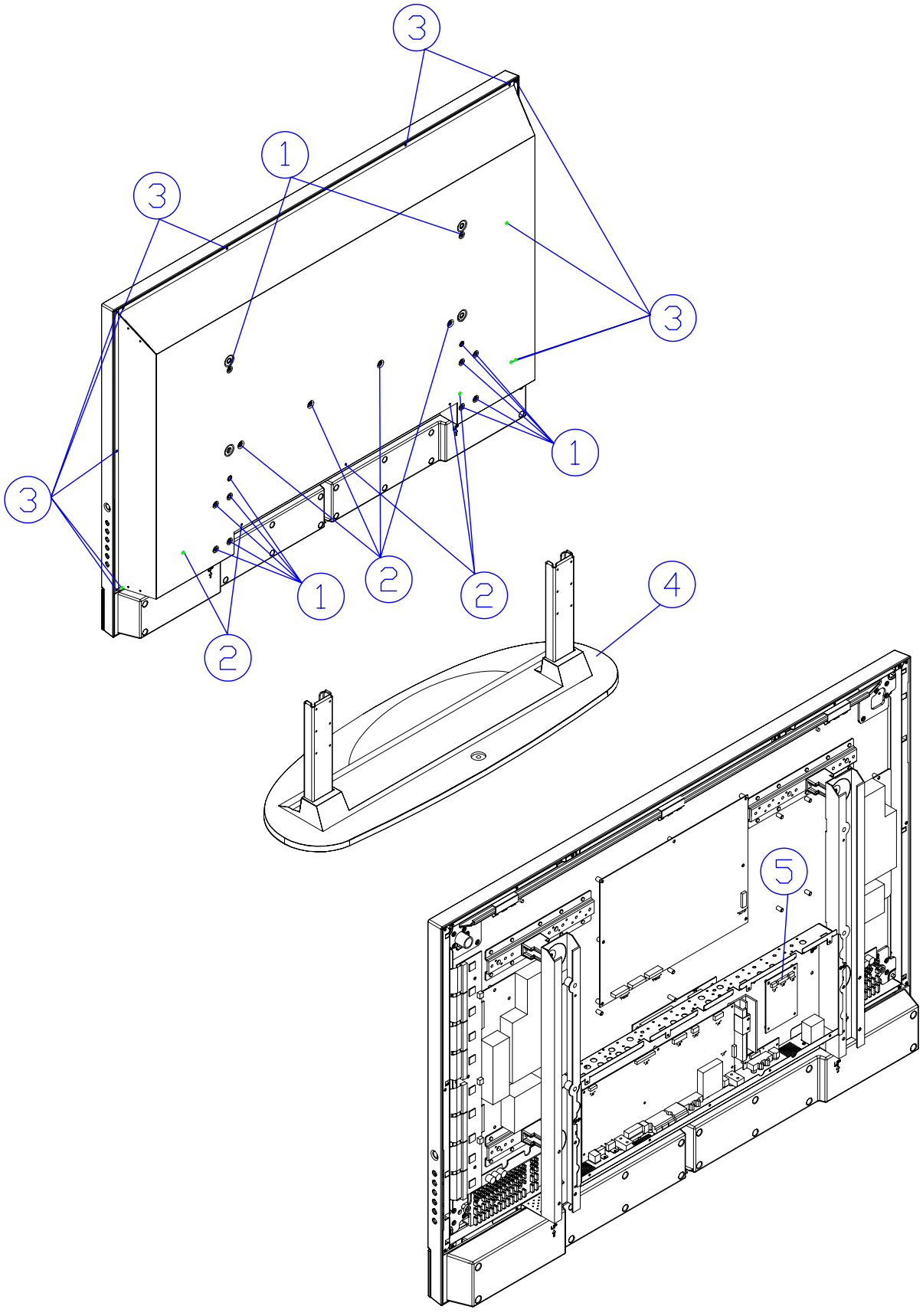
Main Board Block Diagram



1.REAR COVER ASS'Y REMOVAL

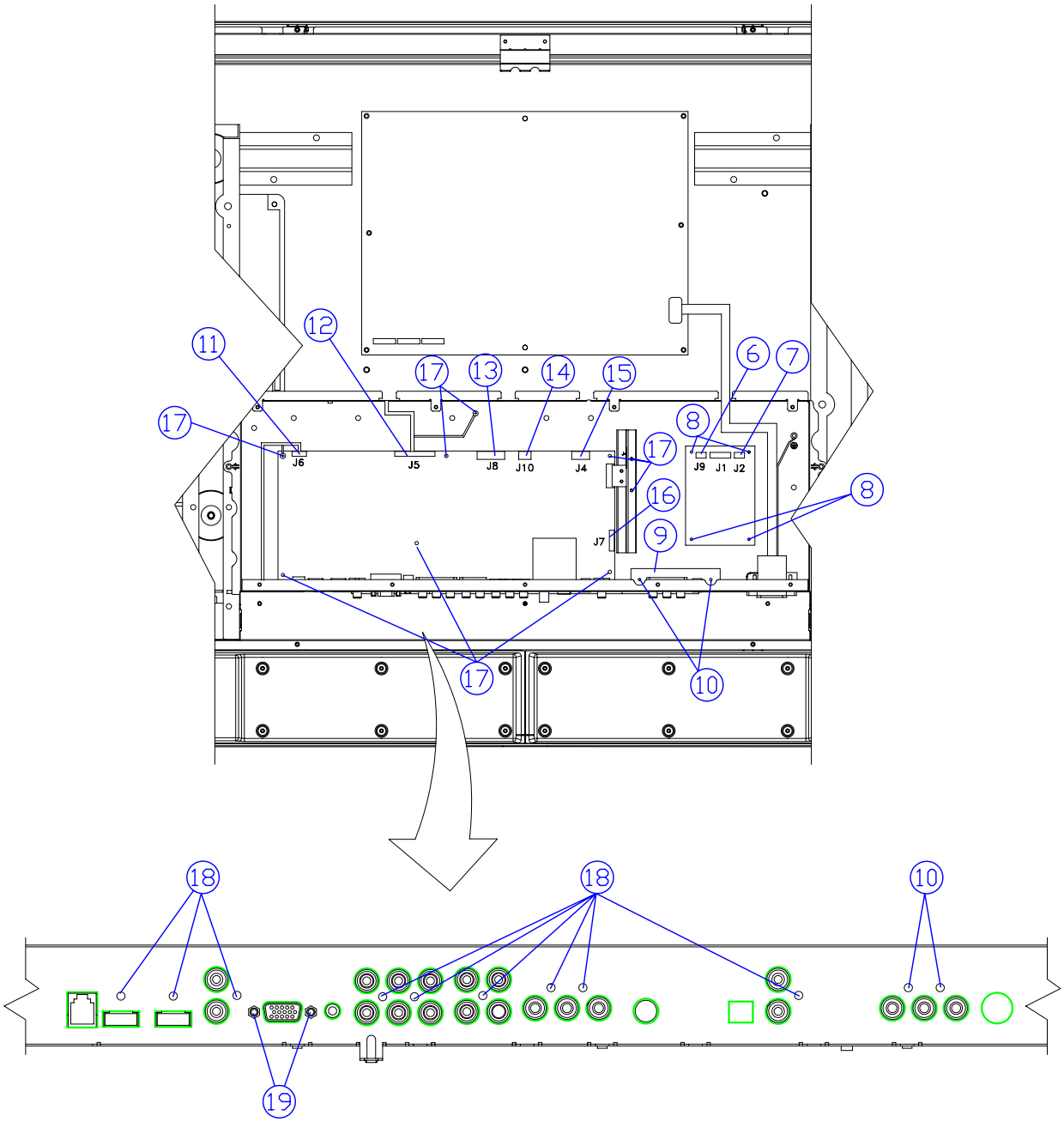
Note:Spread a mat underneath to avoid damaging the Plasama surface.

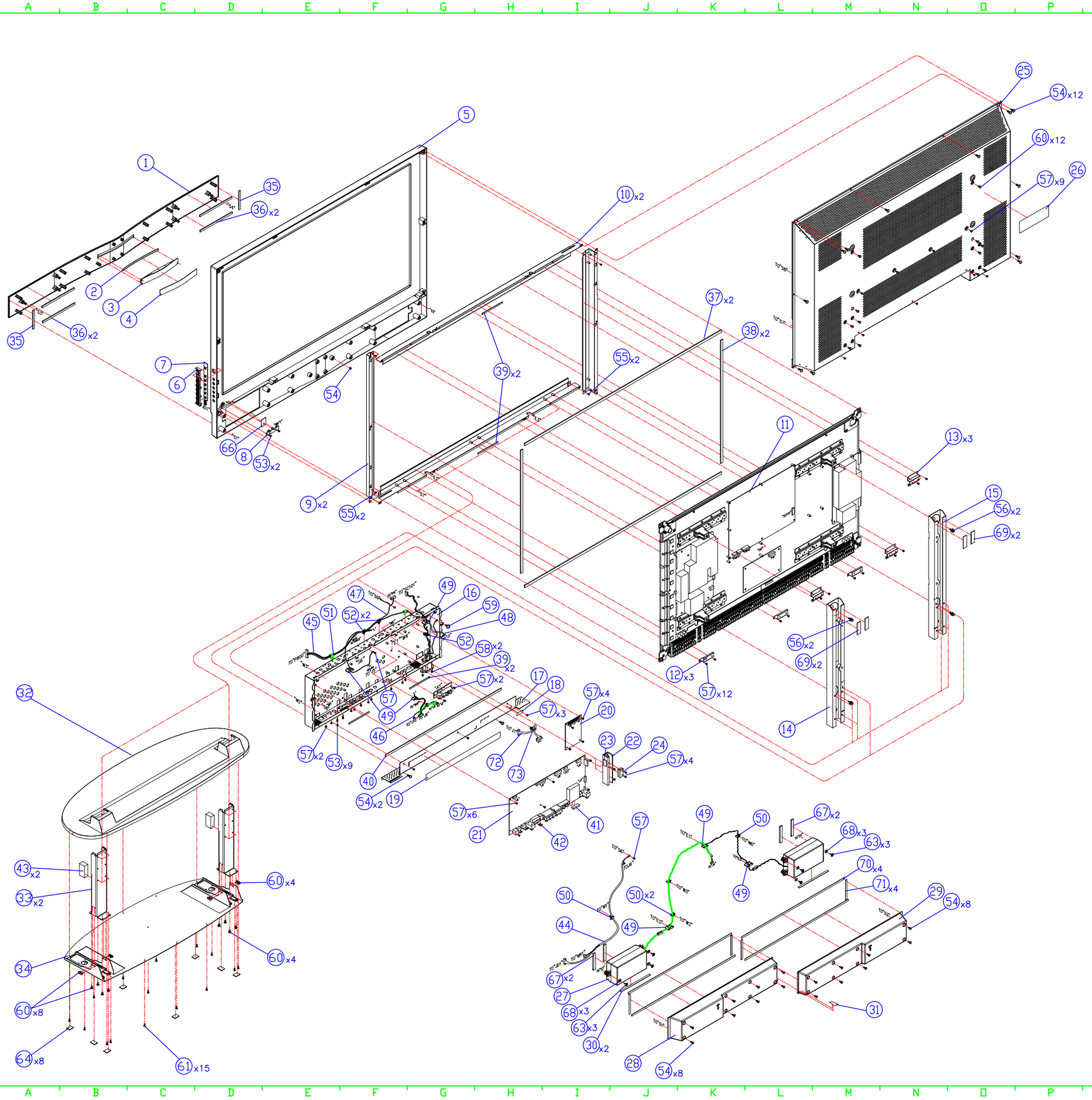
1) Remove twelve screws ① from rear cover.
2) Separate the Base Ass'y ④.
3) Remove nine screws ② and twelve screws ③ from rear cover.
4) Separate the rear cover.
5) Remove the connector ⑤ (J9) of PDP Daughter BD cable.



2. PDP DAUGHTER BD ASS'Y/ MAIN BD ASS'Y/ CONNECTOR BD ASS'Y REMOVAL

1) Disconnector ⑥ (J9) ⑦ (J2) from PDP Daughter BD Ass'y.
2) Remove four screws ⑧.
3) Separate the PDP Daughter BD ASS'Y.
4) Remove the connector ⑨ (JC1) of the connector cable.
5) Remove four screws ⑩ from connector BD Ass'y.
6) Separate the connector BD Ass'y.
7) Remove the connector ⑪ (J6) of the display + IR BD cable.
8) Remove the connector ⑫ (J5) of LVDS cable.
9) Remove two connector ⑬ (J8) ⑭ (J10) of the Daugher BD Ass'y.
10) Remove the connector ⑮ (J4) of the speaker cable.
11) Remove the connector ⑯ (J7) of the connector BD Ass'y.
12) Remove nine screws ⑰ ,nine screws ⑱ and two hexagon screws ⑲ from PCB support.
13) Separate Main BD ASS'Y.





ITEM	PART NO.	DESCRIPTION	QTY
1	1701-1932-3010	SPEAKER NET(VP42 HDTV)(HIPS,877C)	1
2	1701-0800-2230	DECORATION PLATE VIZIO VP42 HDTV	1
3	1701-0811-2060	SPEAKER DECORATION(VP42 HDTV)(PMMA)	1
4	1947-1200-3820	SHINING PLATE(185.0*24.5*0.6T)	1
5	1801-0122-9020	FRONT BEZEL (VP42 HDTV)(ABS,BLACK)ASS'Y	1
6	1701-0416-9010	BUTTON(PD-42FBJ)(ABS,Cr-Plating)	1
7	3820-0062-0156	DISPLAY BD ASS'Y VP42HDTV20A	1
8	3842-0092-0189	PDP IR BD ASS'Y VP42 HDTV 20A	1
9	1712-0101-0660	PANEL BKT_V(VP42 HDTV)(SGCC T=0.8mm)	2
10	1712-0101-0650	PANEL BKT_H(VP42 HDTV)(SGCC T=0.8mm)	2
11	0213-0420-1861	PDP MODULE 42" PDP42X3(LG)(China)(Film type)	1
12	1712-0101-0960	Fix BKT_B(VP42 HDTV)(SECC T=0.8mm)	3
13	1712-0101-0950	Fix BKT_T(VP42 HDTV)(SECC T=0.8mm)	3
14	1712-0101-0630	MAIN FRAME_R(VP42 HDTV)(SGCC T=1.6mm)	1
15	1712-0101-0640	MAIN FRAME_L(VP42 HDTV)(SGCC T=1.6mm)	1
16	1712-0101-1670	PCB SUPPORT(VP42 HDTV20A)(SECC T=0.8mm)	1
17	1712-0200-0720	I/O BKT (VP42 HDTV20A)(SGCC T=0.8mm)	1
18	1701-0800-1540	AC IN PLATE VIZIO P50HDM	1
19	1701-0800-1940	REAR PLATE VIZIO L42 HDTV10A	1
20	3842-0032-0185	PDP Daughter BD ASS'Y VP42 HDTV	1
21	3842-0172-0150	PDP MAIN BD ASS'Y VP42 HDTV 20A	1
22	1712-0400-0720	HEAK SINK(PD-42S)	1
23	1947-1900-0030	HEATPATH (25*14mm)	1
24	1712-0100-4590	HEAT SINK FIX MTEAL(TM-30A)	1
25	1712-0200-0490	REAE COVER(VP42 HDTV)(GGCC T=0.8mm)	1
26	1936-1100-8770	B/C LBL VINC VP42 HDTV	1
27	0335-1006-0750	SPEAKER 10W 6ohm(150*80*55)+Wire 870/610mm(L,R)	1
28	1701-1929-6010	SPEAKER REAR COVER RIGHT (L42 HDTV10A)(HIPS,BLACK)	1
29	1701-1929-6020	SPEAKER REAR COVER LEFT (L42 HDTV10A)(HIPS,BLACK)	1
30	1947-1500-3150	SPENGE(146L*7W*0.5t)(VP42)	2
31	1947-1200-3420	Masking Mylar(13*25mm,t=0.25MM)	1
32	1701-0524-4010	BASE COVER(VP42 HDTV)(ABS,877C)	1
33	1712-0101-0740	BASE FRAME(VP42 HDTV)(SECC T=2.0mm)	2
34	1712-0100-8991	BASE PLATE(PD-42L)(SECC T1.2/ø 6mm)	1
35	1947-1500-3020	SPONGE(80.0*7.0*3.0t)	2
36	1947-1500-3030	SPONGE(160.0*7.0*3.0t)	4
37	1947-1800-1200	GASKET BLOCK(980.0L*10.0W*3.0H)	2
38	1947-1800-1210	GASKET BLOCK(530.0L*10.0W*3.0H)	2
39	1947-1800-0240	GASKET EMI(5*1*100mm)	4
40	1947-1800-0990	GASKET BLOCK L576*W8*H2mm(PD-42L)	1
41	1947-1800-0370	GASKET BLOCK(5.5H*10.0W*30.0Lmm)	1
42	1947-1800-0490	GASKET BLOCK(12L*10W*2.5Hmm)HOLE 6 ø	1
43	1947-1800-0980	GASKET BLOCK L50*W17*H25(PD42FB)	2
44	0460-1008-0501	WH A2001H02-8P/A2001H02-4P+5P UL20276#28 795/700mm	1
45	0460-1015-0130	WH A2001-15P/5P+A2512H00-13P 1007#24 160/320+CORE	1
46	0460-1005-0560	WH A2001H02-5P/A2001H02-4P 1007#24 220mm	1
47	0460-4131-0040	WH FI-W31S/P240430 UL20276#30 340 mm Core*2	1
48	0460-1110-0070	WH A2512H00-10P/A2501H02-8P 1007#22 410mm+CORE	1
49	1701-1500-1080	EDGE SADDLE DS-12(NYLON)	6
50	1701-1500-0220	WIRE SADDLE(CH-02)	5
51	1701-1500-1350	WIRE CLIP(TDY8-1A)	2
52	1701-1500-1570	WIRE SADDLE(CM-10M)(GV46L HDTV)	3
53	1721-0003-0650	TAP.SCREW-TB #3.0*6.0L,BLK-Ni	11
54	1721-0003-1250	TAP.SCREW-TB#3.0*12.0L,BLK-Ni	31
55	1720-0003-0320	Screw,M-3*3mm	4
56	1720-2505-1020	MAC.SCREW-MR M5.0*10L,Ni	4
57	1720-0003-0650	MAC.SCREW-MB M3.0*6.0L,BLK-Ni	46
58	1720-3003-0850	MAC.SCREW-MF M3.0*8.0L,BLK-Ni	2
59	1720-1204-0820	MAC.SCREW-MPGW M4.0*8.0L,Ni	1
60	1720-0004-0850	MAC.SCREW-MB M4.0*8.0L,BLK-Ni	28
61	1721-3003-0920	TAP.SCREW-MF M3.0*9.0L,Ni	15
62	1720-7344-0820	MAC.SCREW-MHSW #4-40*8.0L,Ni	2
63	1721-4103-1220	TAP.SCREW-TRF#3.0*12.0L,Ni	6
64	1701-1000-0520	FOOT(PORON)(20mm*15mm/2.0mm)(PD-42L)	8
65	0320-4000-0142	POWER CORD 110V UL/CSA 1800mm BLK(VINC)	1
66	1947-1800-1310	GASKET BLOCK(22.0L*30.0W*1.0H)	1
67	1947-1500-3140	SPENGE(70L*10W*4t)(VP42)	4
68	1701-1300-0140	WASHER(PC 12D*3.5D*0.8t)(VP42)	6
69	1947-1500-3190	Poron(50L*16.5W*1.7t)(VP42)	4
70	1947-1500-3160	SPENGE(515L*7W*0.5t)(VP42)	4
71	1947-1500-3170	SPENGE(85L*7W*0.5t)(VP42)	4
72	0460-1012-0260	WHA2001H02-12P/A2001H02-12P 1061#26 150mm	1
73	1701-1500-0450	WIRE SADDLE(CH-01P)	1
74	3632-0022-0146	CONNECTOR BD ASS'Y VX32L HDTV	1

	VIZIO VP42HDTV 20A		9842-8500-5053
	DESCRIPTION		PART NO.
	AmTRAN TECHNOLOGY Co., LTD.	THIRD ANGLE PROJECTION	MODEL No: VIZIO VP42HDTV 20A(LC)
UNLESS OTHERWISE NOTED	DSN: Jessie Yu 04/10/07	MATERIAL:	DWG. NAME: 42" CASE ASS'Y
XX = ±0.10	CHK:	QTY: 1 SIZE: A1	
X = ±0.2		SCALE: Full UNIT: MM	DWG. No: VIZIO-VP42HDTV-20A-LC.DWG REV. 0 SHEET: 1 of 1
ANG. = ±1/2°			